Phase Control Thyristor
Type T193-2500-52

High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current	I_{TAV}	2500 A
Repetitive peak off-state voltage	V_{DRM}	4600 ÷ 5200 V
Repetitive peak reverse voltage	V_{RRM}	
Turn-off time	t_q	800 μs

V_{DRM}, V_{RRM}, V	4600	4800	5000	5200
Voltage code	46	48	50	52
T_j, °C	– 60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	2500 3900	T_c= 98 °C, Double side cooled T_c= 70 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	3925	T_c= 98 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	55.0 63.0	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			58.0 67.0	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
I^2t	Safety factor	$A^2s \cdot 10^3$	15100 19800	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			13900 18600	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600÷5200	$T_{j\ min}$< T_j <$T_{j\ max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700÷5300	$T_{j\ min}$< T_j <$T_{j\ max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	T_j=$T_{j\ max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	12	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ µs; $di_G/dt \geq 2$ A/µs
THERMAL				
T_{stg}	Storage temperature	°C	-60 ÷ 50	
T_j	Operating junction temperature	°C	-60 ÷ 125	
MECHANICAL				
F	Mounting force	kN	70.0 ÷ 90.0	
a	Acceleration	m/s^2	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	2.10	$T_j=25$ °C; $I_{TM}=6300$ A
$V_{T(TO)}$	On-state threshold voltage, max	V	1.00	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$
r_T	On-state slope resistance, max	mΩ	0.190	
I_L	Latching current, max	mA	1500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ µs; $di_G/dt \geq 1$ A/µs
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/µs	500, 1000, 1600	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	5.00 3.00 2.00	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$ $V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$ $V_D=12$ V; $I_D=3$ A; Direct gate current
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current
I_{GD}	Gate non-trigger direct current, min	mA	15.00	
SWITCHING				
t_{gd}	Delay time	µs	4.00	$T_j=25$ °C; $V_D=1500$ V; $I_{TM}=I_{TAV}$; $di/dt=200$ A/µs; Gate pulse: $I_G=2$ A; $V_G=20$ V; $t_{GP}=50$ µs; $di_G/dt=2$ A/µs
t_q	Turn-off time[2], max	µs	800	$dv_D/dt=50$ V/µs; $T_j=T_{j\,max}$; $I_{TM}=1000$ A; $di_R/dt=-5$ A/µs; $V_R=100$ V; $V_D=1600$ V;
Q_{rr}	Total recovered charge, max	µC	12500	$T_j=T_{j\,max}$; $I_{TM}=1000$ A; $di_R/dt=-5$ A/µs; $V_R=100$ V
t_{rr}	Reverse recovery time, typ	µs	157	
I_{rrM}	Peak reverse recovery current, max	A	159	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0050	Direct current	Double side cooled
R_{thjc-A}			0.0110		Anode side cooled
R_{thjc-K}			0.0090		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0010	Direct current	
MECHANICAL					
w	Weight, max	g	2200		
D_s	Surface creepage distance	mm (inch)	44.60 (1.756)		
D_a	Air strike distance	mm (inch)	15.70 (0.618)		

PART NUMBERING GUIDE

T	193	2500	52	A2	B2	N
1	2	3	4	5	6	7

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage, V/µs
6. Turn-off time (dv_D/dt=50 V/µs)
7. Ambient conditions: N – normal; T – tropical

NOTES

1) Critical rate of rise of off-state voltage

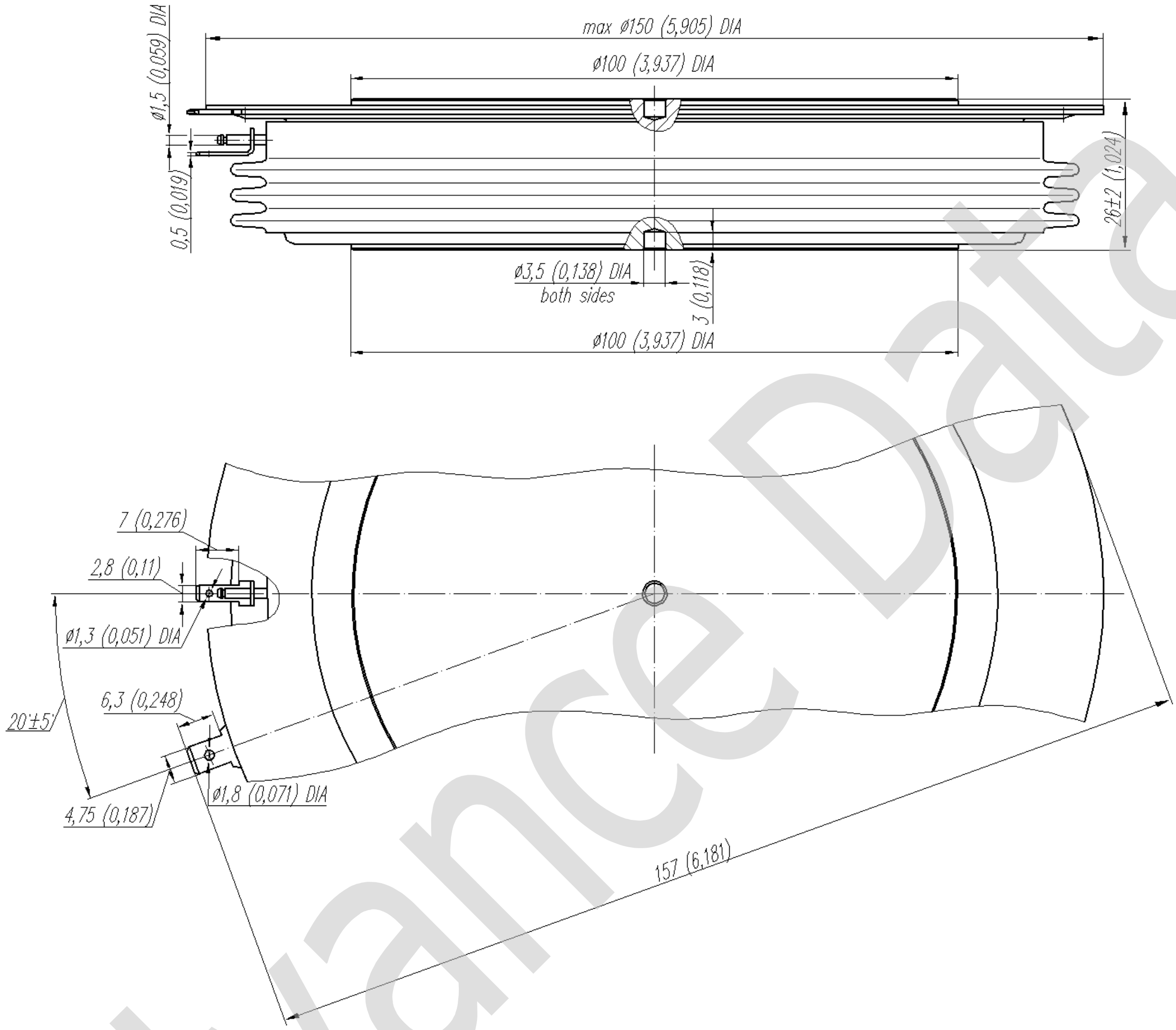
Symbol of Group	E2	A2	T1
$(dv_D/dt)_{crit}$, V/µs	500	1000	1600

2) Turn-off time (dv_D/dt=50 V/µs)

Symbol of Group	B2
t_q, µs	800

OVERALL DIMENSIONS

Package type: T.G5



All dimensions in millimeters (inches)

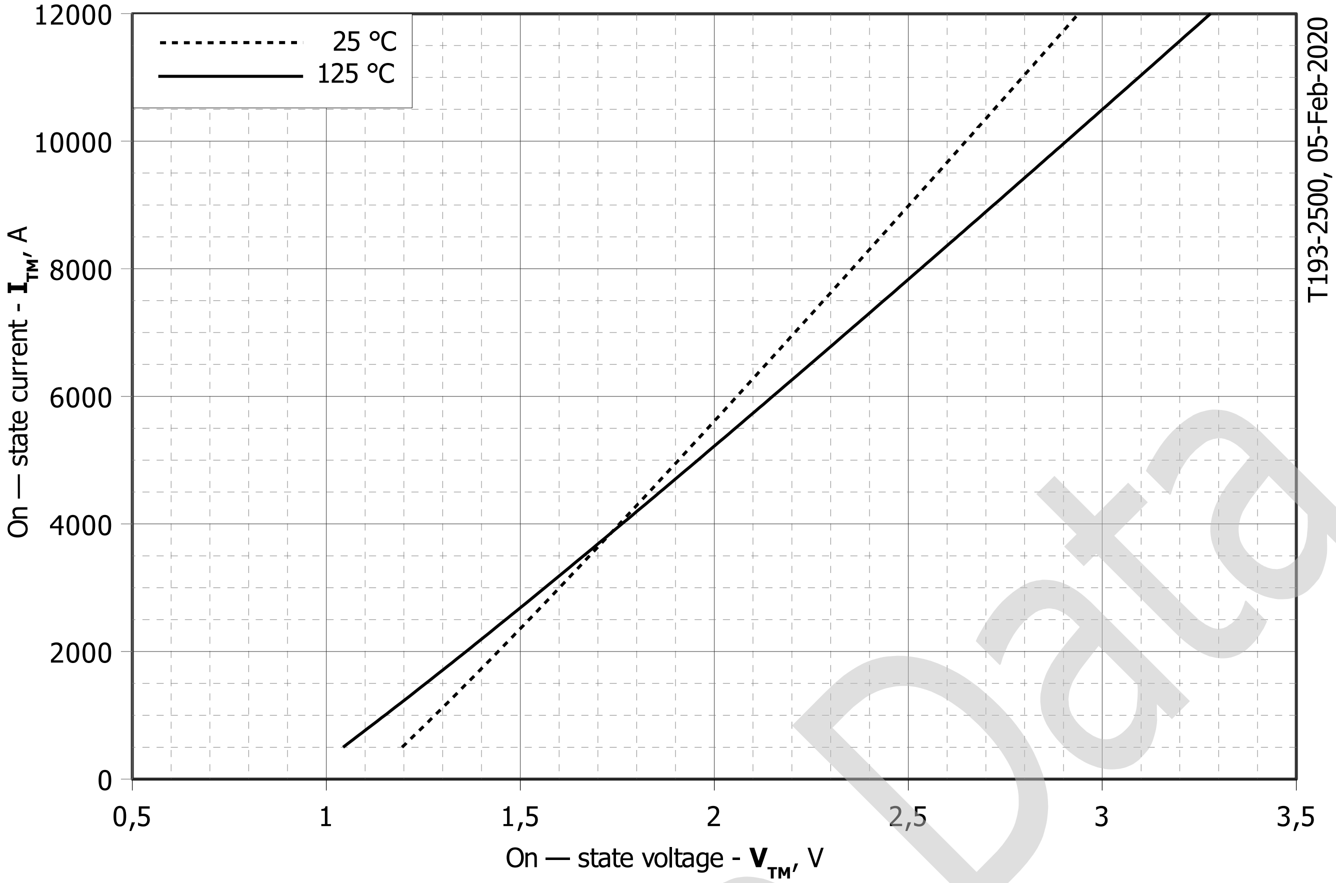


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	$T_j = T_{j\,max}$
A	1.17300000	1.04510000
B	0.00012979	0.00016438
C	-0.01979700	-0.03193100
D	0.00360030	0.00512580

On-state characteristic model (see Fig. 1)

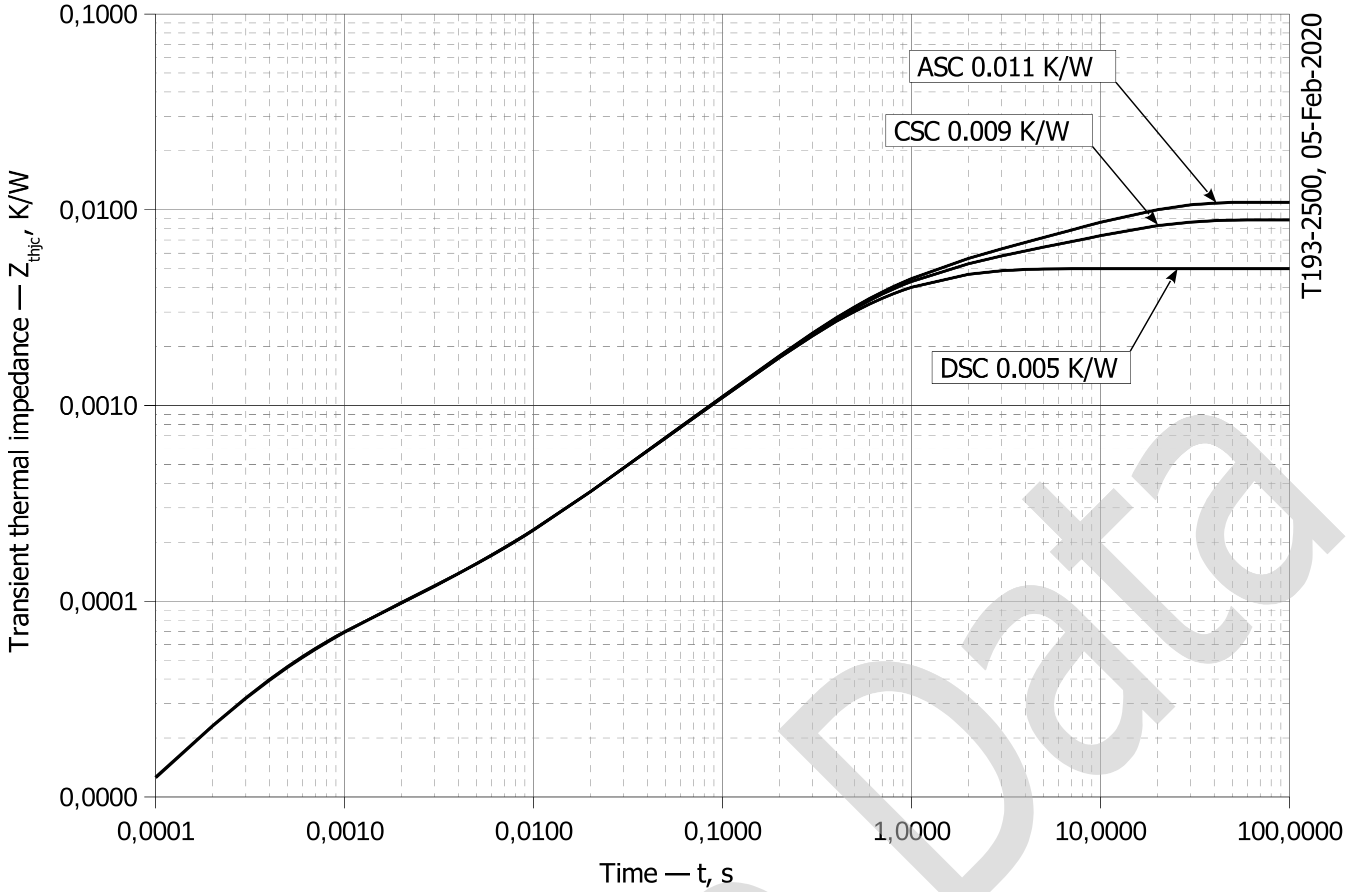


Fig 2 – Transient thermal impedance Z_{thjc} vs. time t

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i, K/W	0.002027	0.0001166	0.002627	0.0001539	3.237e-005	4.335e-005
τ_i, s	1.059	0.080	0.3836	0.02289	0.0003559	0.001397

DC Anode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.005945	0.002218	0.00248	0.0002153	3.862e-005	4.604e-005
τ_i, s	10.6	1.120	0.3786	0.03196	0.002513	0.0004352

DC Cathode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.003885	0.002188	0.002508	0.0002154	3.854e-005	4.646e-005
τ_i, s	10.6	1.090	0.3745	0.03207	0.002565	0.0004383

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

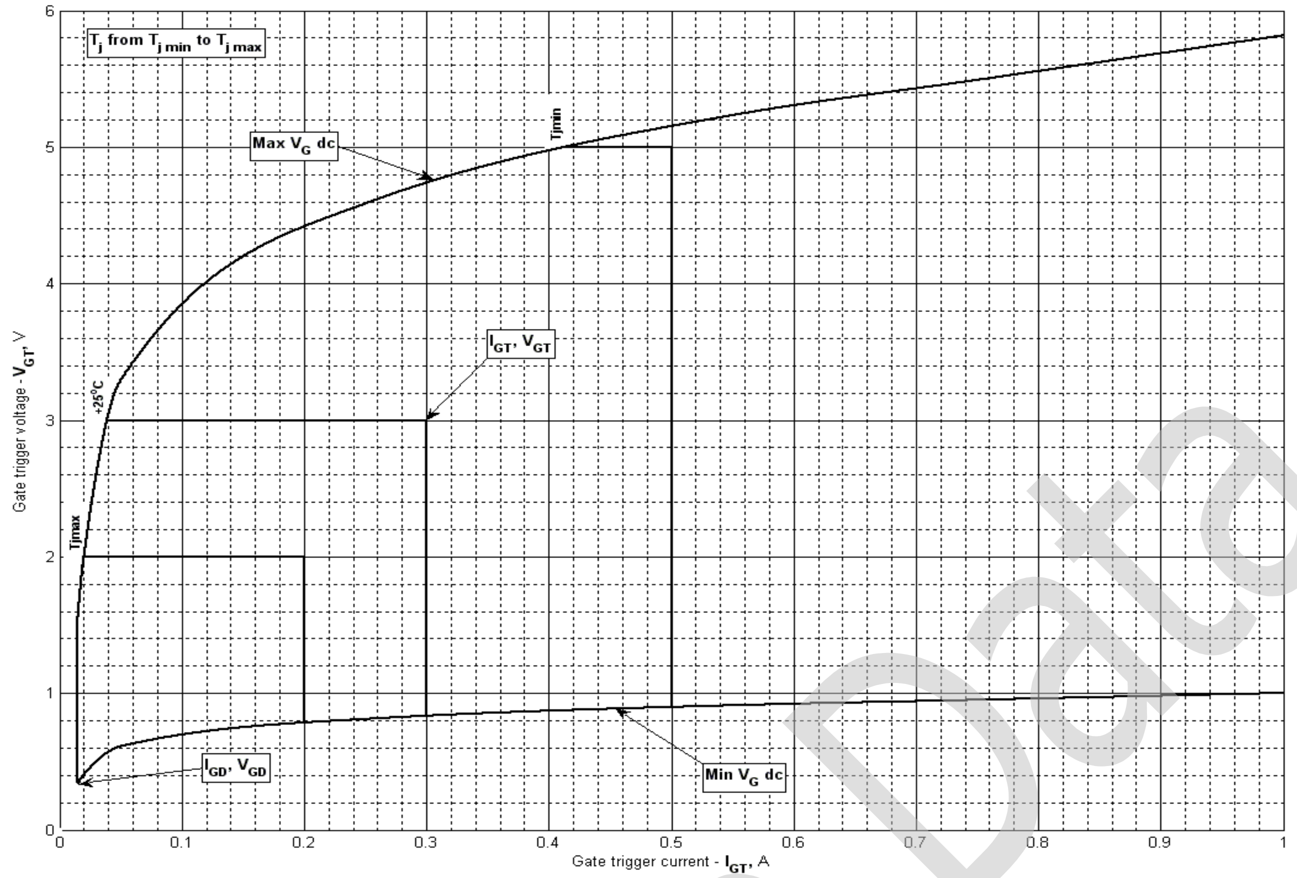


Fig 3 – Gate characteristics – Trigger limits

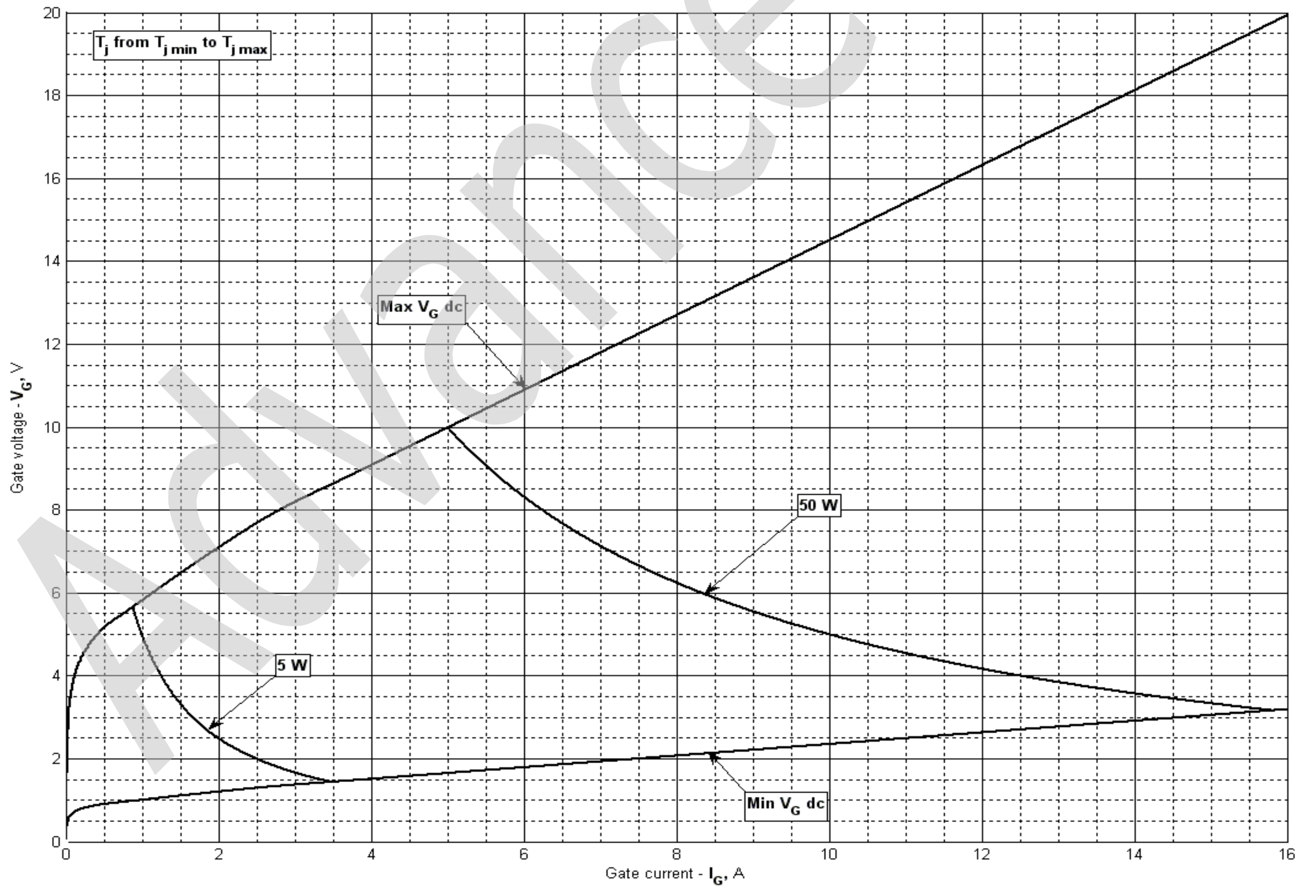


Fig 4 - Gate characteristics – Power curves

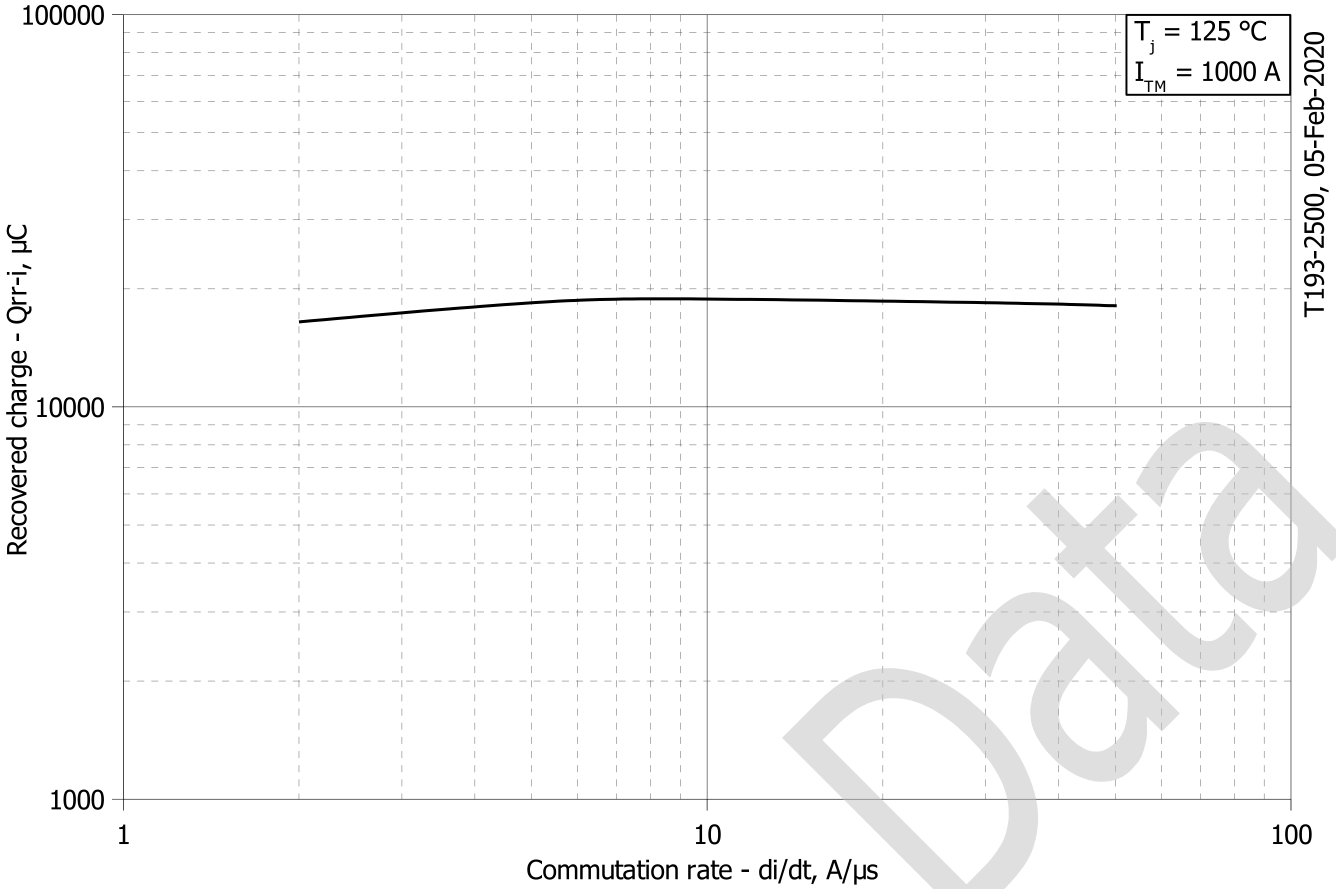


Fig 5 – Maximum recovered charge Q_{rr-i} (integral) vs. commutation rate di_R/dt

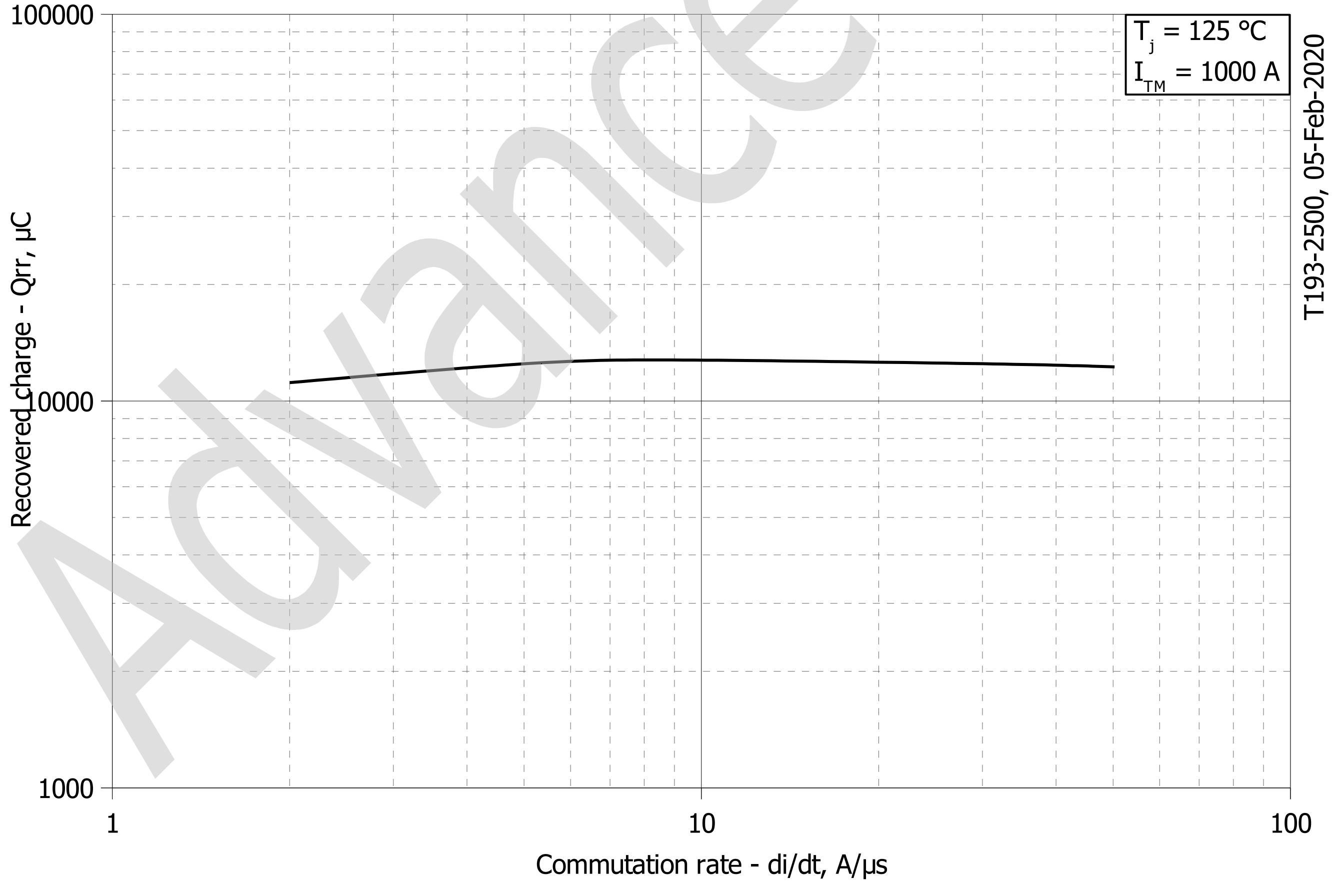


Fig 6 – Maximum recovered charge Q_{rr} vs. commutation rate di_R/dt (25% chord)

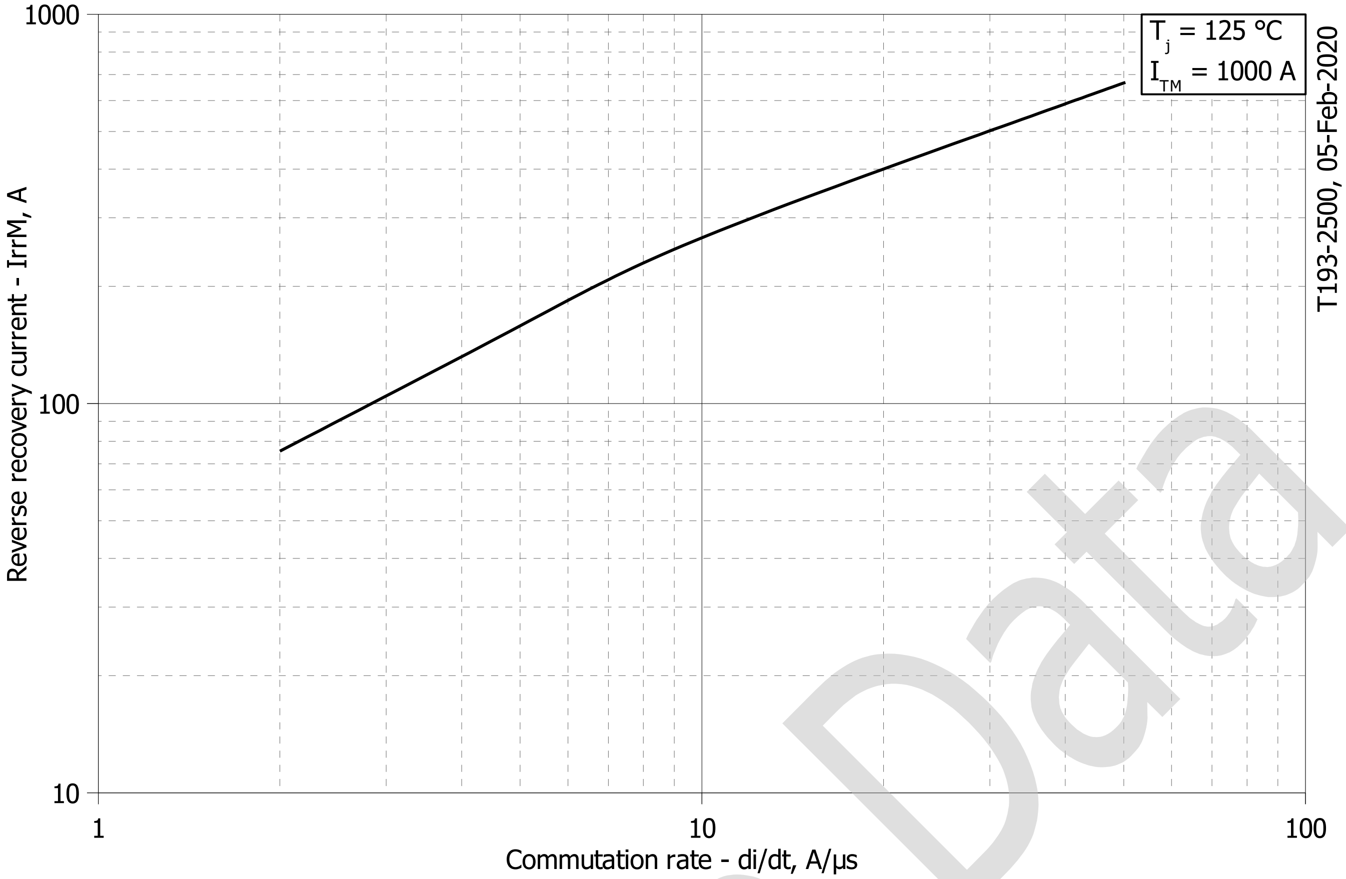


Fig 7 – Maximum reverse recovery current I_{rrM} vs. commutation rate di_R/dt

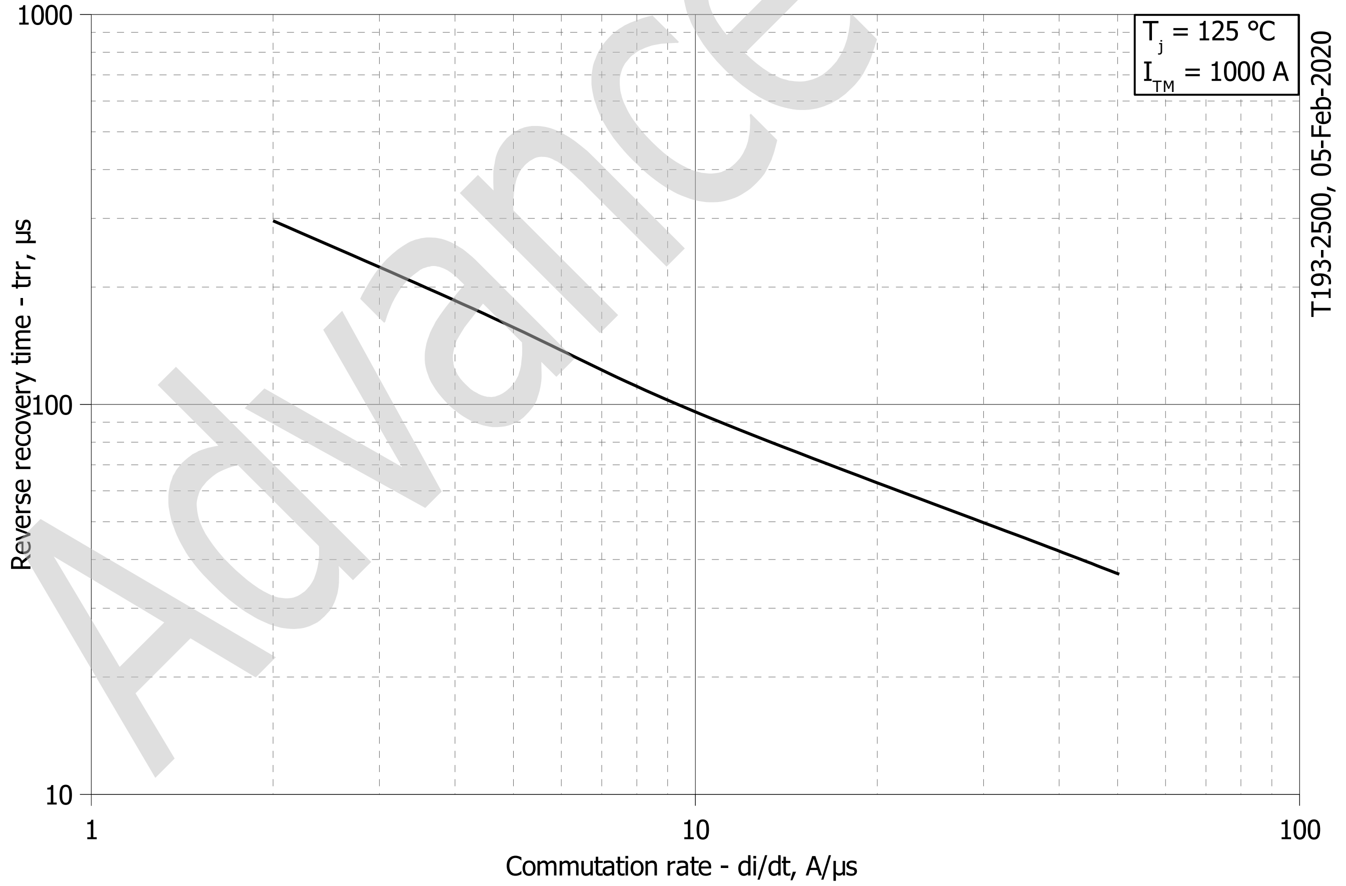


Fig 8 – Maximum recovery time t_{rr} vs. commutation rate di_R/dt (25% chord)

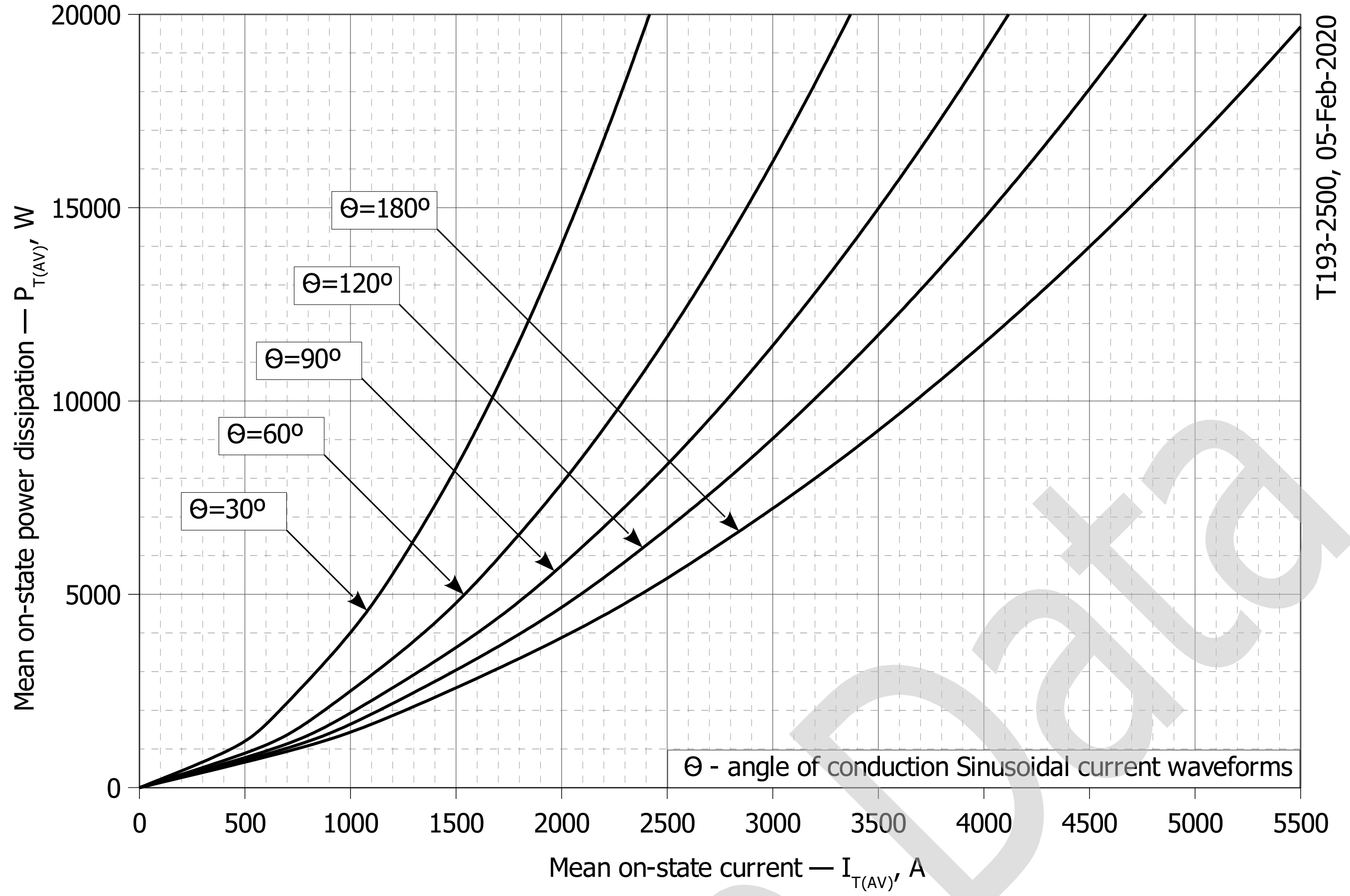


Fig. 9 - Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

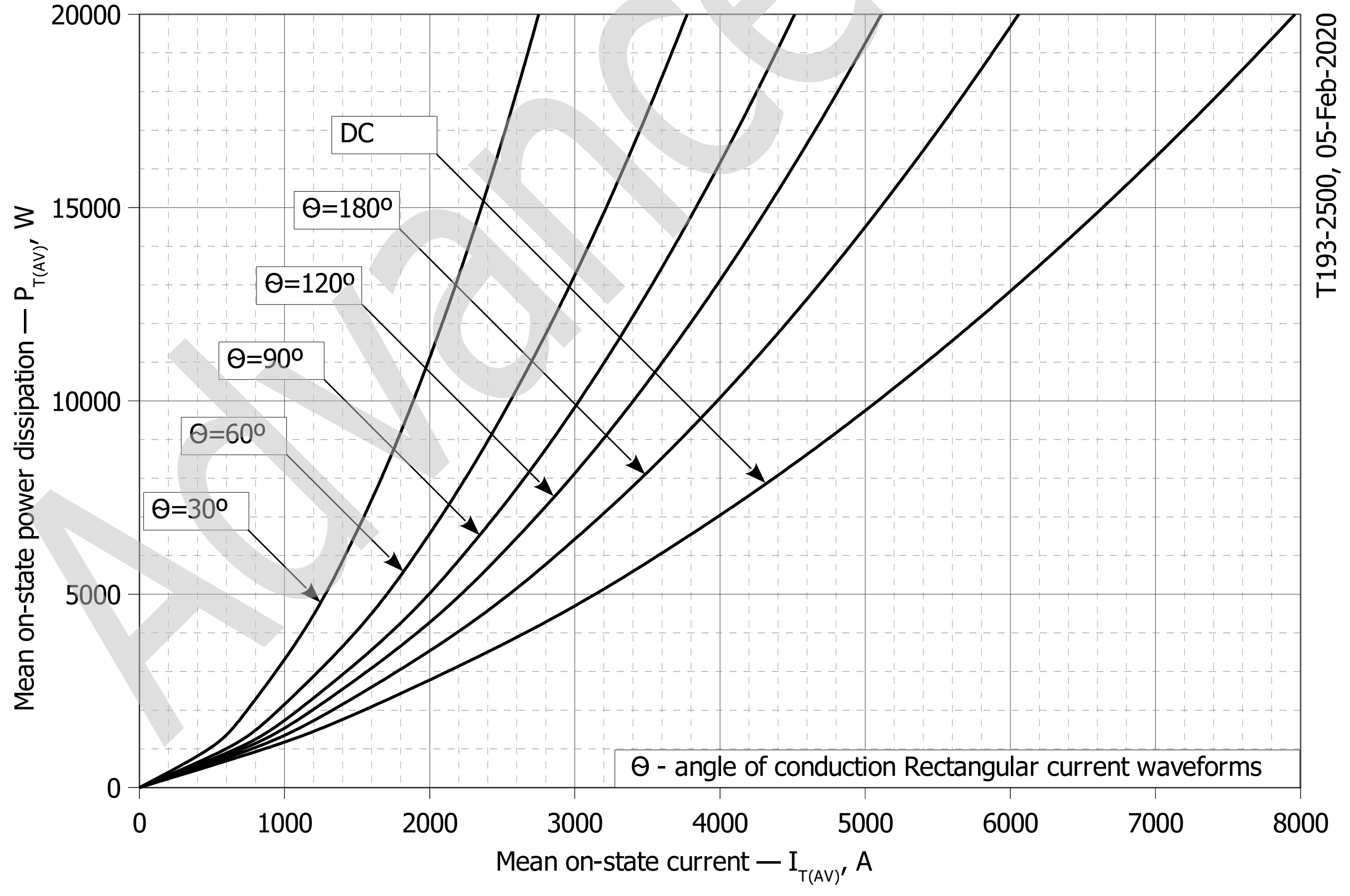


Fig. 10 – Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

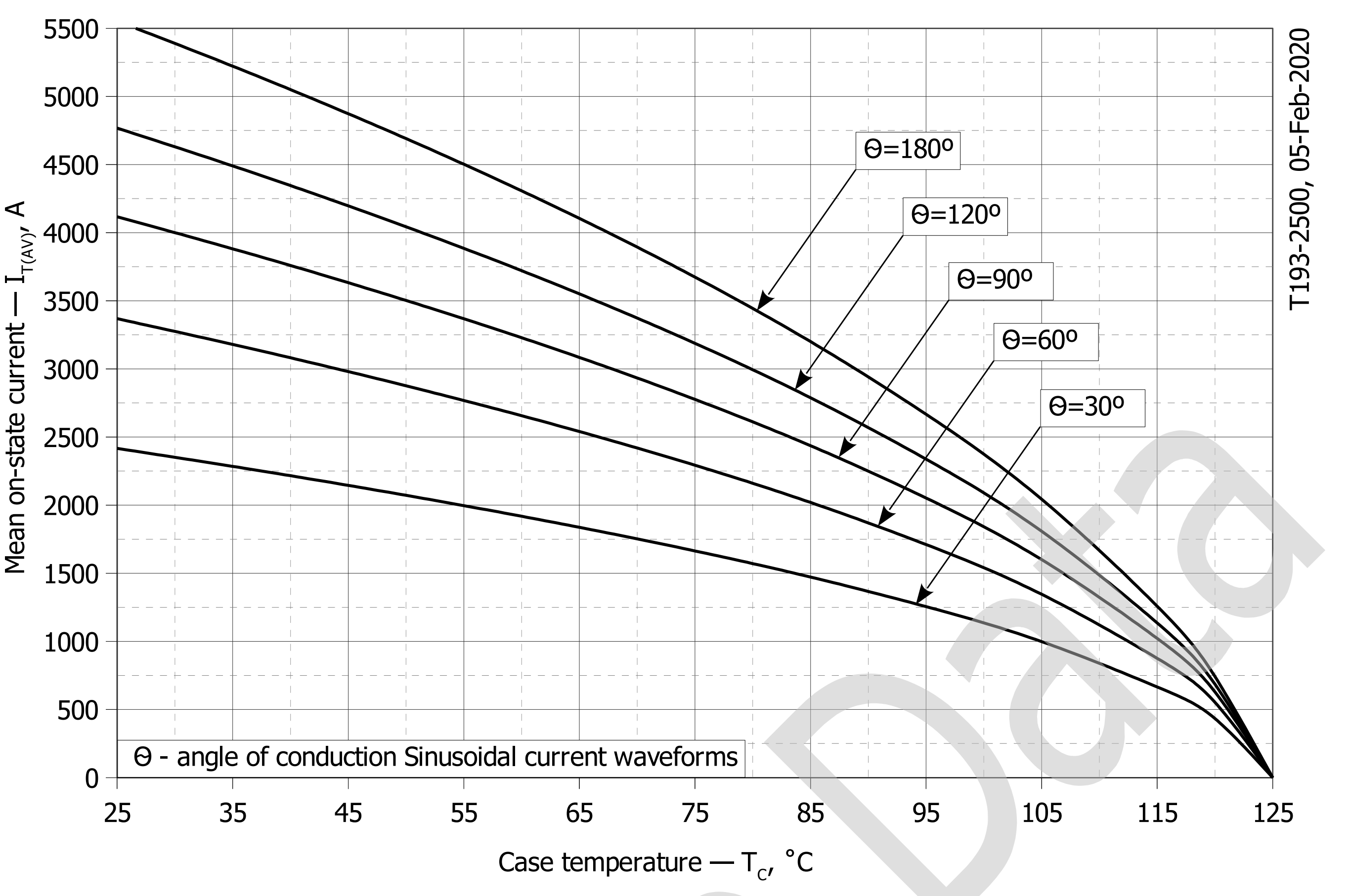


Fig. 11 – Mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

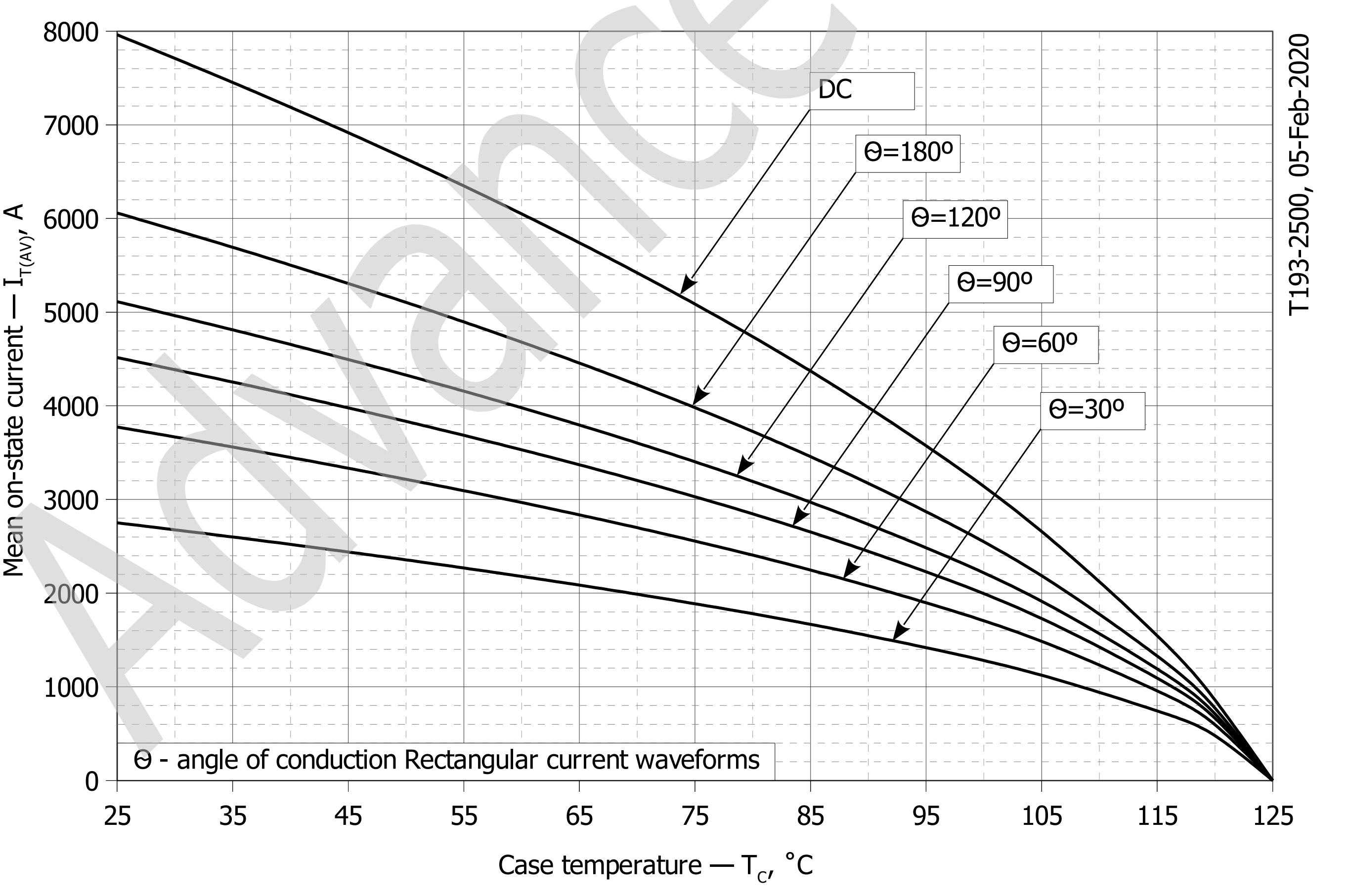


Fig. 12 - Mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

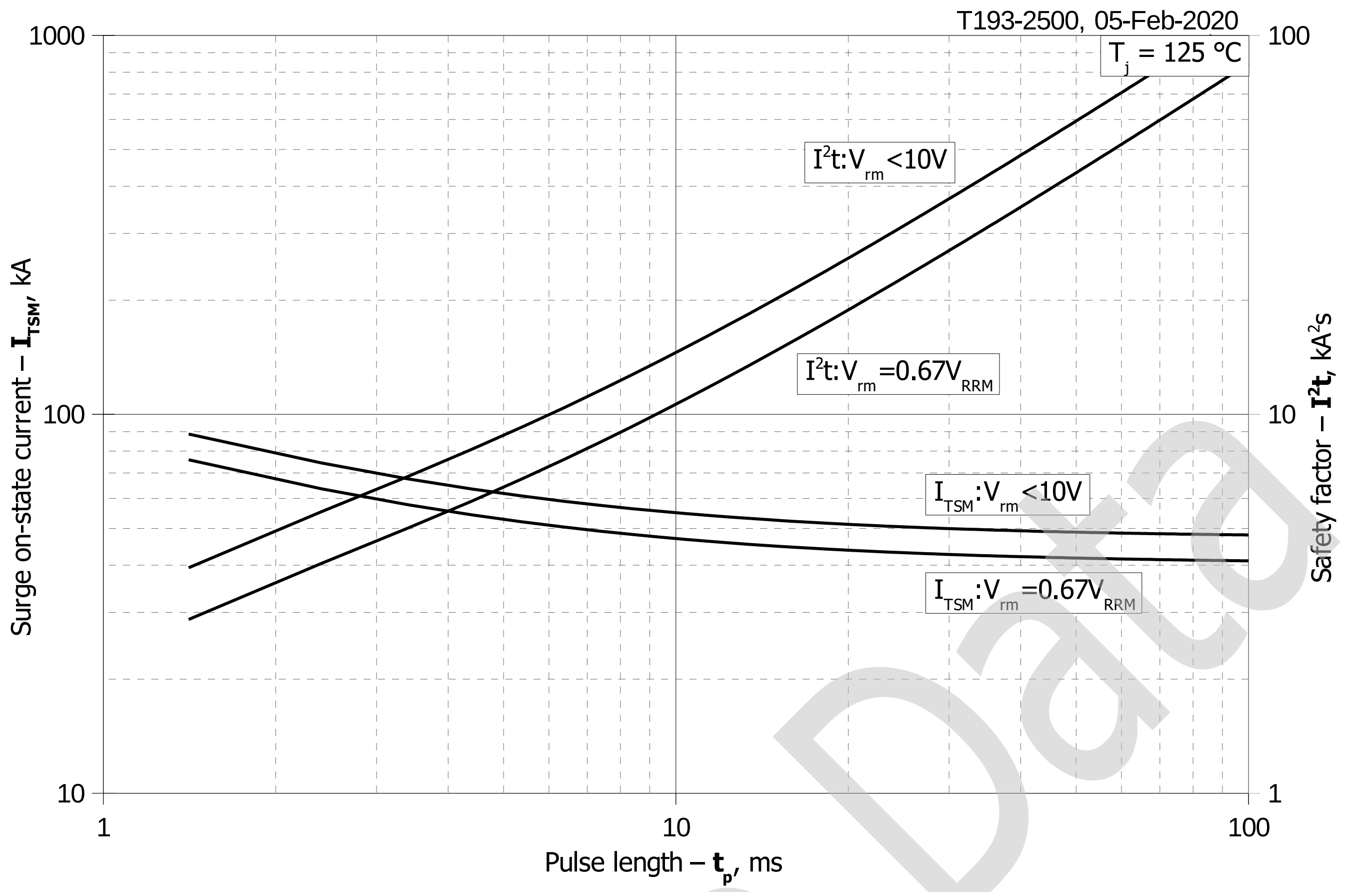


Fig. 13 – Maximum surge on-state current I_{TSM} and safety factor I^2t vs. pulse length t_p

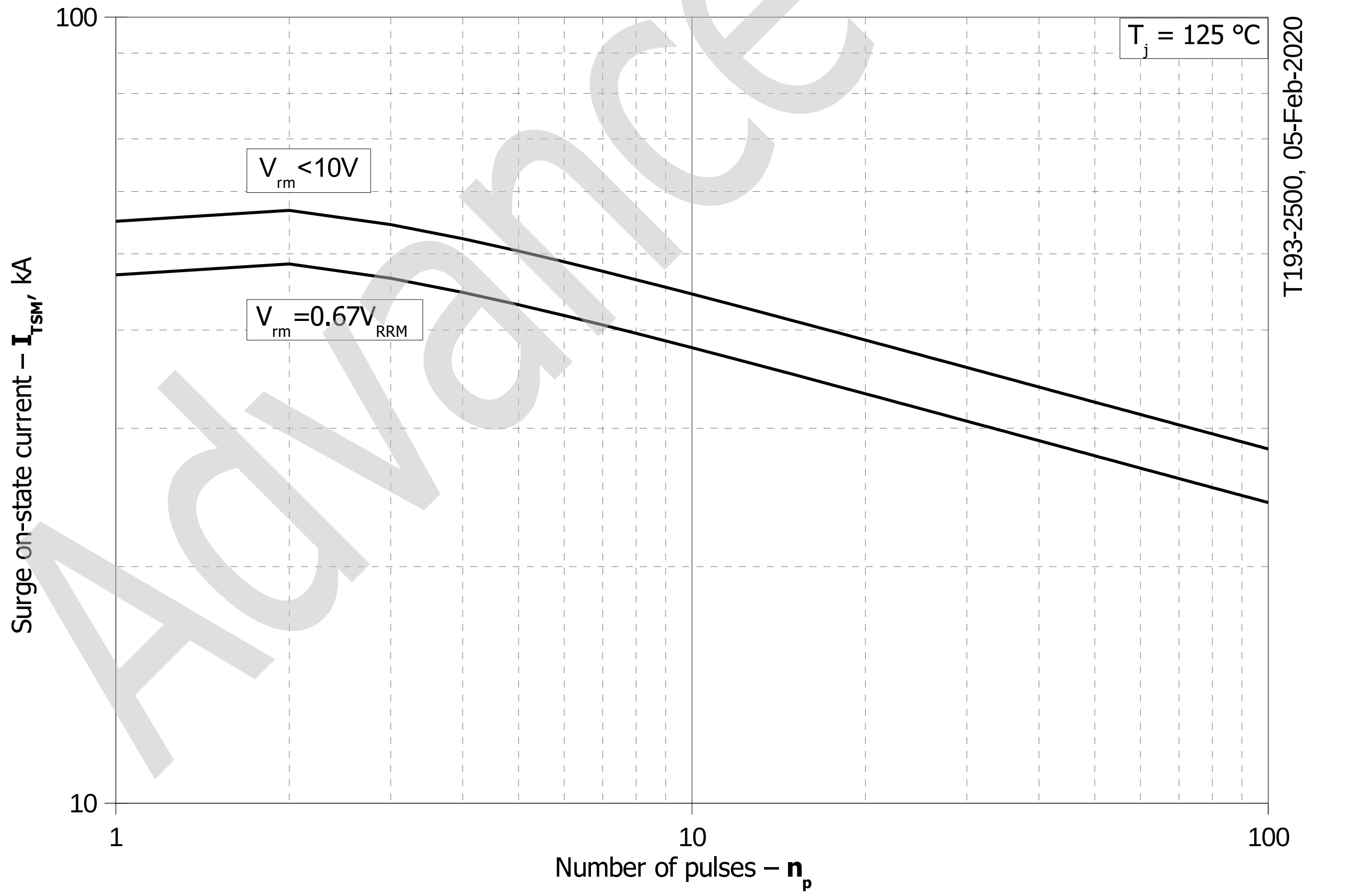


Fig. 14 - Maximum surge on-state current I_{TSM} vs. number of pulses n_p