



High power cycling capability
Low on-state and switching losses
Designed for traction and industrial applications

Phase Control Thyristor Type T183-3200-28

Mean on-state current	I_{TAV}		3200 A		
Repetitive peak off-state voltage	V_{DRM}		2000 ÷ 2800 V		
Repetitive peak reverse voltage	V_{RRM}				
Turn-off time	t_q		400 μ s		
V_{DRM}, V_{RRM}, V	2000	2200	2400	2600	2800
Voltage code	20	22	24	26	28
$T_j, ^\circ C$	- 60 ÷ 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	3200 3340 4111	$T_c = 87^\circ C$, Double side cooled $T_c = 85^\circ C$, Double side cooled $T_c = 70^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	5024	$T_c = 87^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	60.0 69.0	$T_j = T_{j\max}$ $T_j = 25^\circ C$ 180° half-sine wave; 50 Hz ($t_p = 10$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
			63.0 72.0	$T_j = T_{j\max}$ $T_j = 25^\circ C$ 180° half-sine wave; 60 Hz ($t_p = 8.3$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2 \cdot s \cdot 10^3$	18000 23805	$T_j = T_{j\max}$ $T_j = 25^\circ C$ 180° half-sine wave; 50 Hz ($t_p = 10$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
			16470 21510	$T_j = T_{j\max}$ $T_j = 25^\circ C$ 180° half-sine wave; 60 Hz ($t_p = 8.3$ ms); single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000 ÷ 2800	$T_{j\min} < T_j < T_{j\max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100 ÷ 2900	$T_{j\min} < T_j < T_{j\max}$; 180° half-sine wave; 50 Hz; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75 · V_{DRM} 0.75 · V_{RRM}	$T_j = T_{j\max}$; Gate open

TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	630	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2 I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 \div 125	
T_j	Operating junction temperature	$^{\circ}$ C	-60 \div 125	
MECHANICAL				
F	Mounting force	kN	60.0 \div 70.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

CHARACTERISTICS

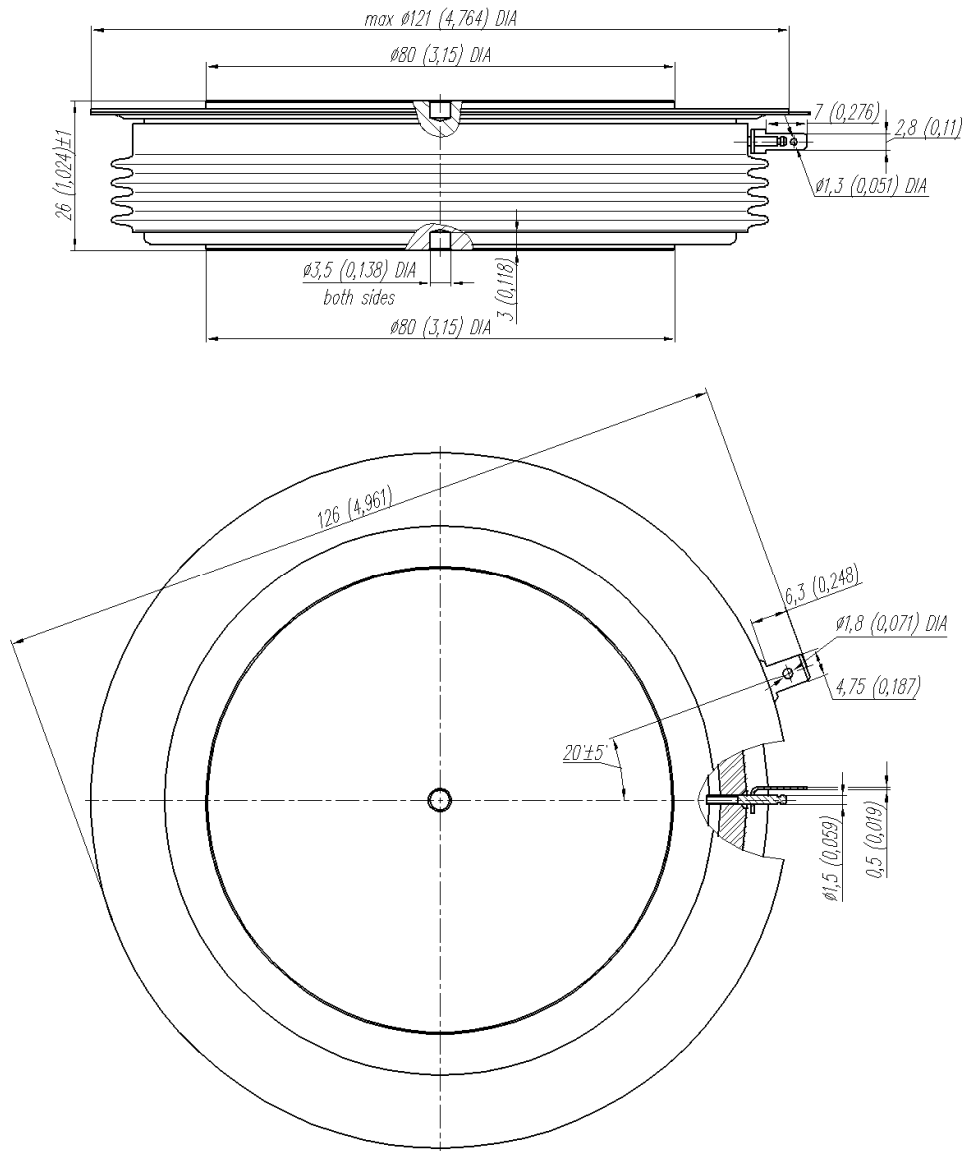
Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.55	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 6300$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.90	$T_j = T_{j\ max}$;	
r_T	On-state slope resistance, max	m Ω	0.115	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j = T_{j\ max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	1000	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00	$T_j = T_{j\ min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\ max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			3.00		
I_{GT}	Gate trigger direct current, max	mA	500	$T_j = T_{j\ min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\ max}$	
			300		
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j = T_{j\ max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	15.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	4.00	$T_j = 25$ $^{\circ}$ C; $V_D = 0.4 \cdot V_{DRM}$; $I_{TM} = 2000$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	400	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}$; $I_{TM} = 2000$ A; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 V_{DRM}$;	
Q_{rr}	Total recovered charge, max	μ C	4000	$T_j = T_{j\ max}$; $I_{TM} = 2000$ A;	
t_{rr}	Reverse recovery time, max	μ s	53	$di_R/dt = -5$ A/ μ s;	
I_{rrM}	Peak reverse recovery current, max	A	150	$V_R = 100$ V	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0065	Direct current	Double side cooled
R_{thjc-A}			0.0143		Anode side cooled
R_{thjc-K}			0.0117		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0015	Direct current	
MECHANICAL					
w	Weight, typ	g	1900		
D_s	Surface creepage distance	mm (inch)	36.50 (1.437)		
D_a	Air strike distance	mm (inch)	16.5 (0.650)		

PART NUMBERING GUIDE

T	183	3200	28	N
1	2	3	4	5

1. Phase Control Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Ambient conditions: N – normal; T – tropical



All dimensions in millimeters (inches)

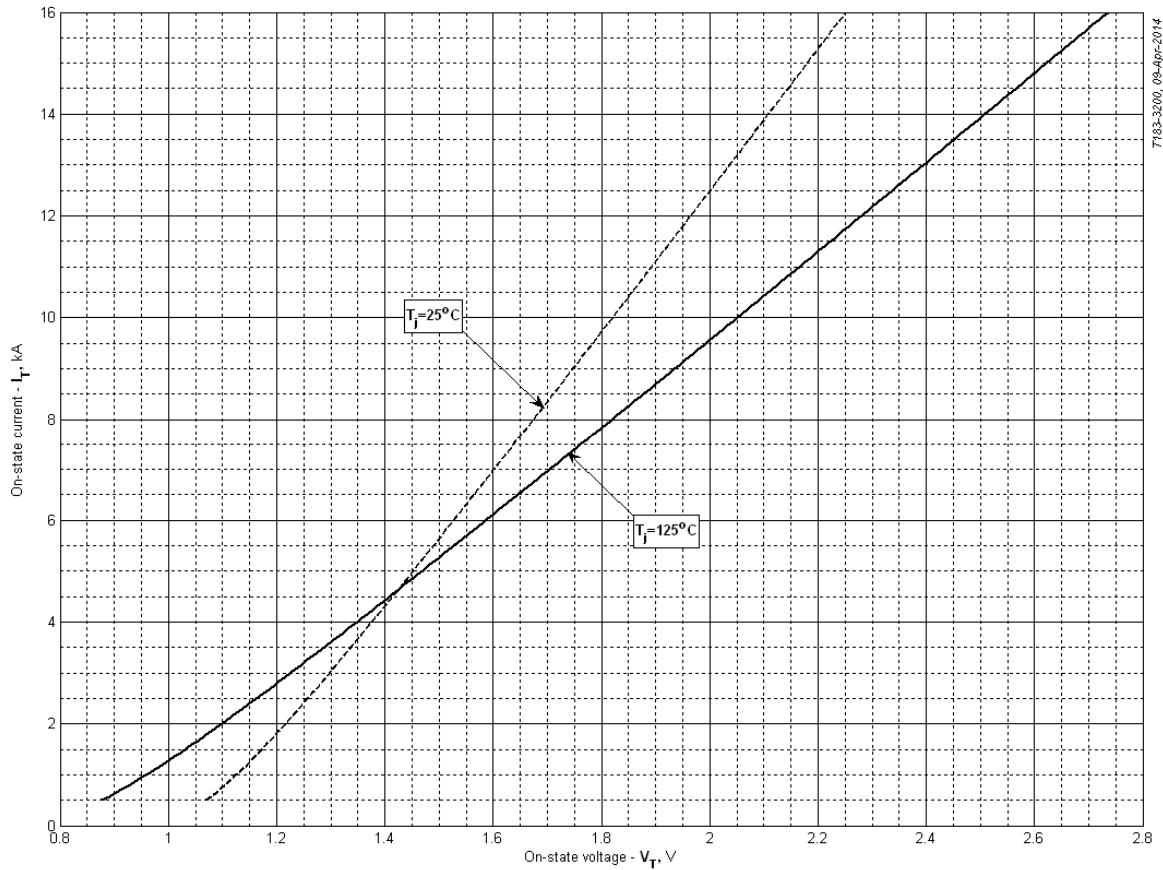


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	$T_j = 25^\circ\text{C}$	$T_j = T_{j,\text{max}}$
A	1.069448	0.866423
B	0.079099	0.123820
C	0.164566	0.219790
D	-0.137520	-0.183667

On-state characteristic model (see Fig. 1)

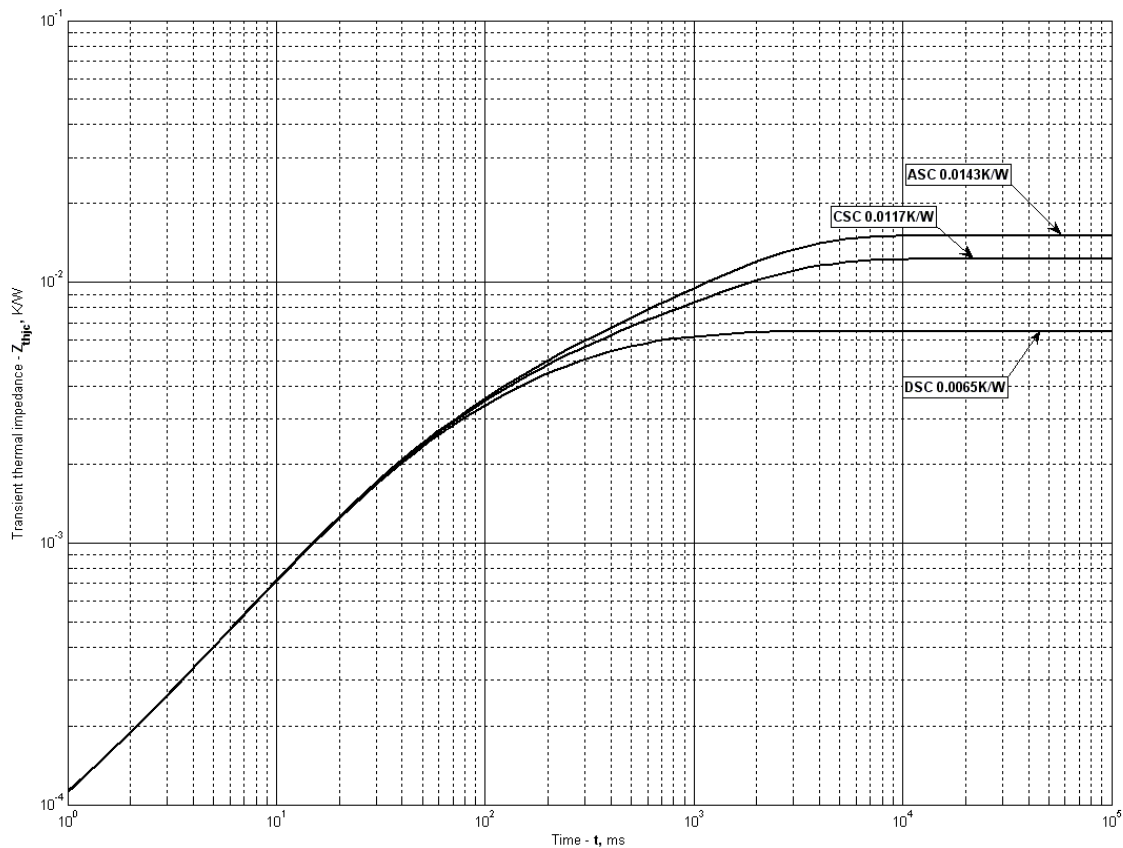


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^n R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where $i = 1$ to n , n is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t .

R_i = Amplitude of p_{th} term.

τ_i = Time constant of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i K/W	0.001031	0.003117	0.001895	0.0004176	2.061e-005	1.999e-005
τ_{ij} s	0.7345	0.209	0.05291	0.01652	0.0006764	0.0002168

DC Cathode side cooled

i	1	2	3	4	5	6
R_i K/W	0.001475	0.005797	0.002722	0.001822	0.0003923	3.824e-005
τ_{ij} s	0.8755	1.835	0.1997	0.05221	0.01594	0.0003499

DC Anode side cooled

i	1	2	3	4	5	6
R_i K/W	0.00848	0.001792	0.002597	0.00179	0.0003904	3.851e-005
τ_{ij} s	1.845	0.9581	0.2011	0.05234	0.01605	0.0003606

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

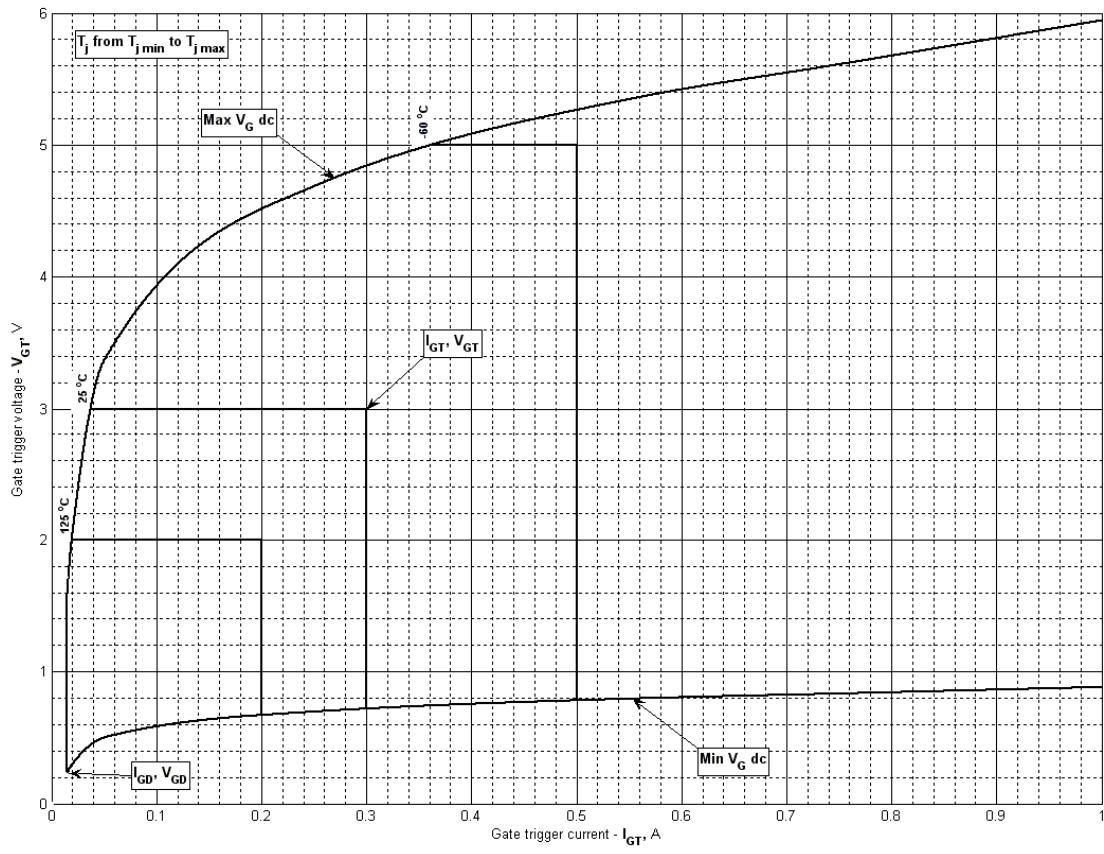


Fig 3 – Gate characteristics – Trigger limits

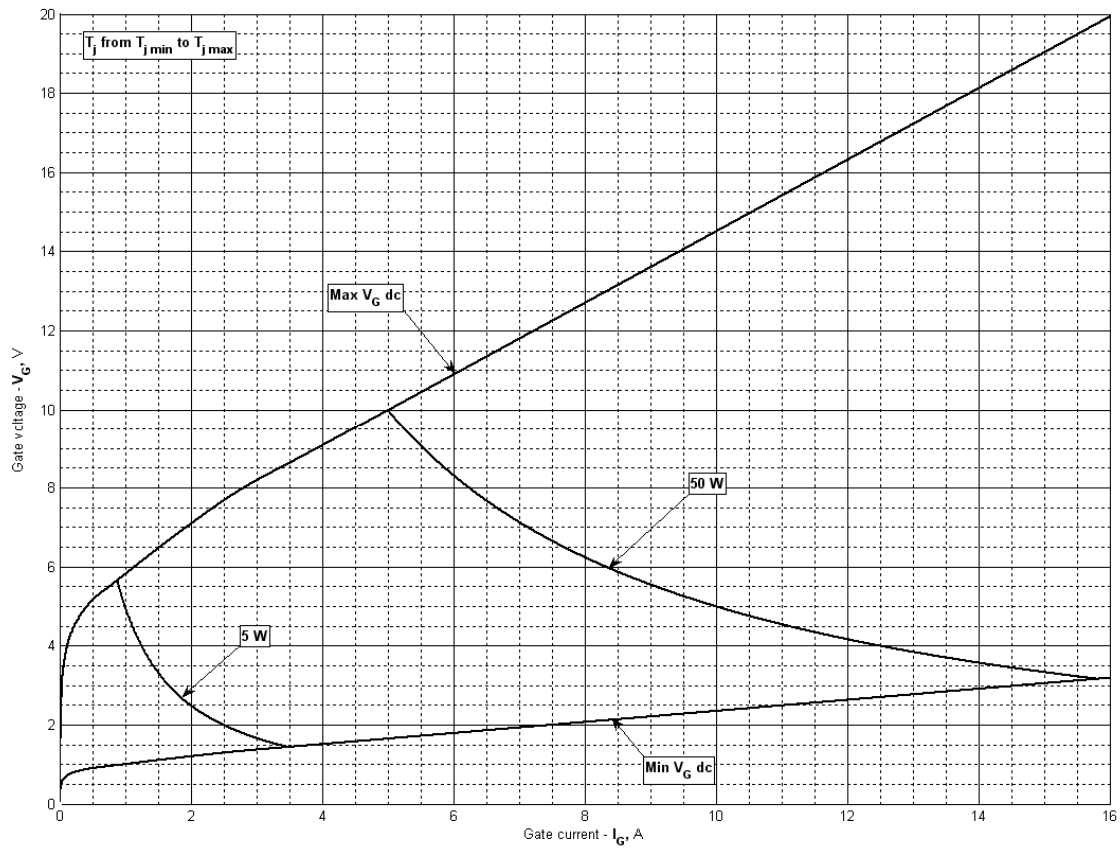


Fig 4 - Gate characteristics – Power curves

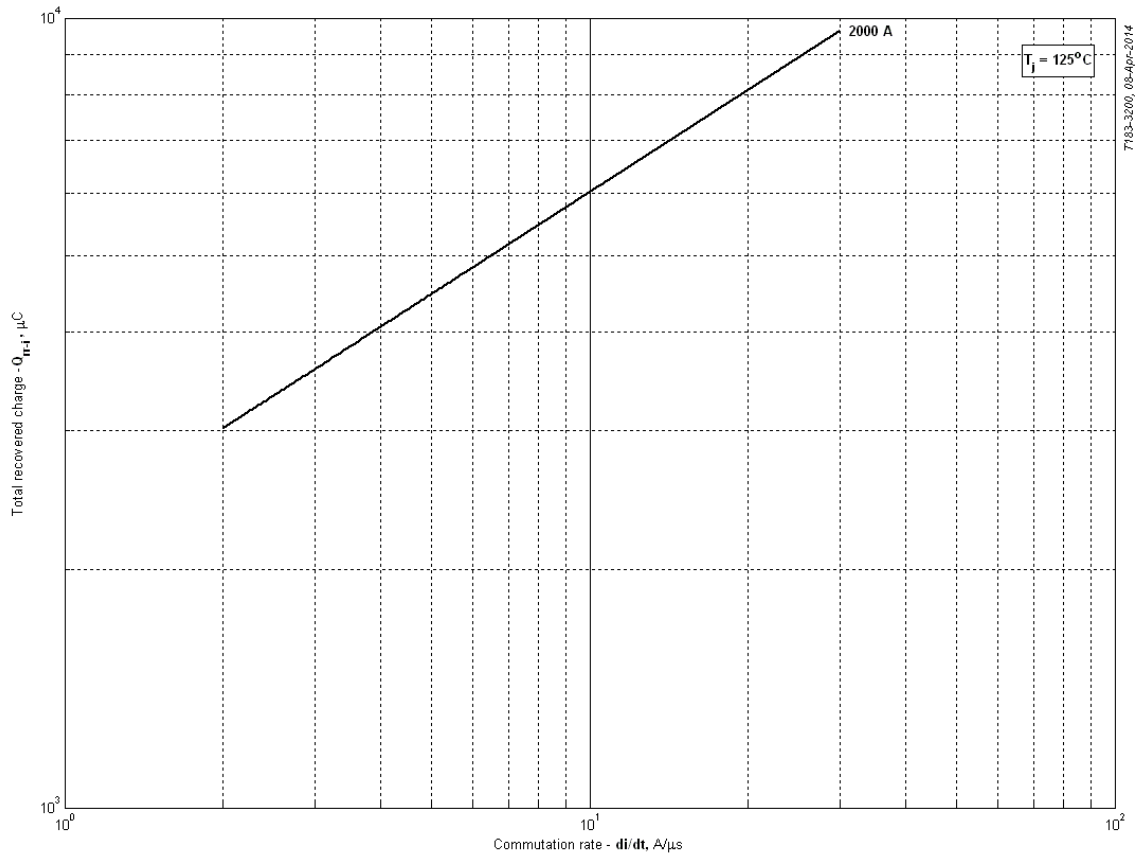


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

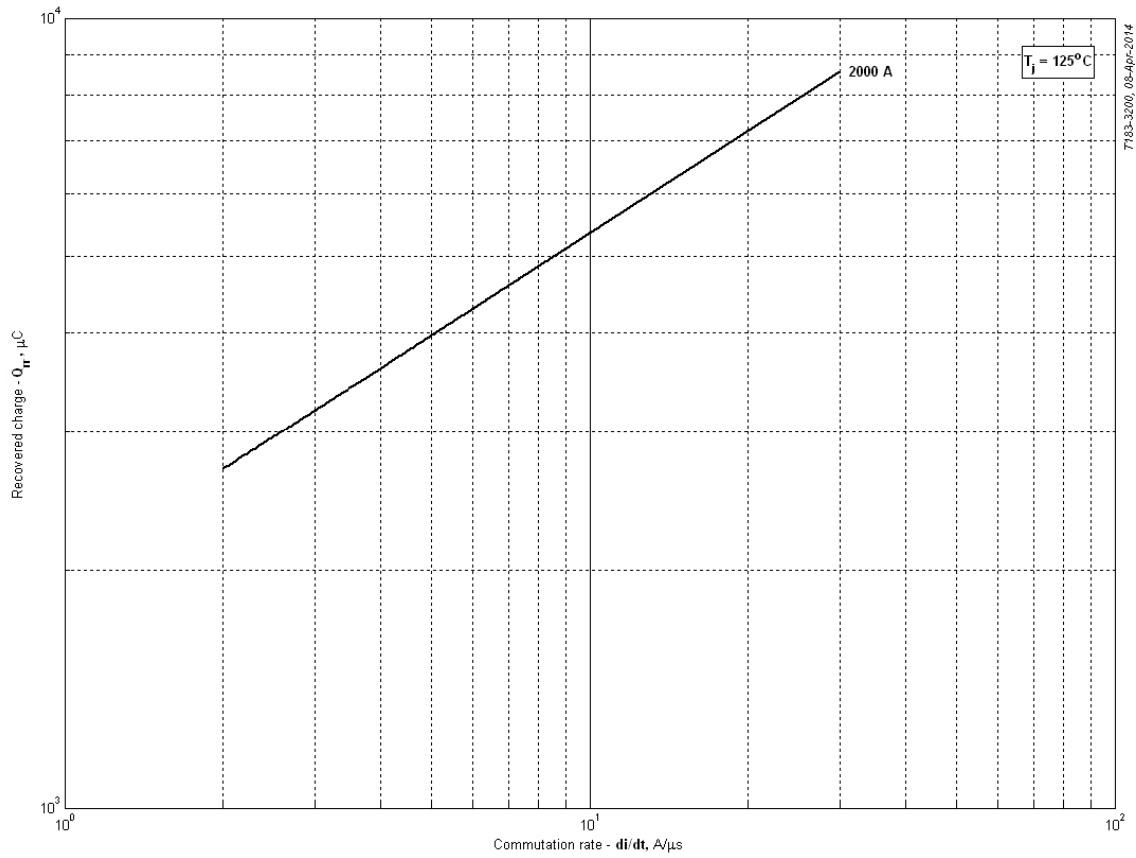


Fig 6 - Recovered charge, Q_{rr} (linear)

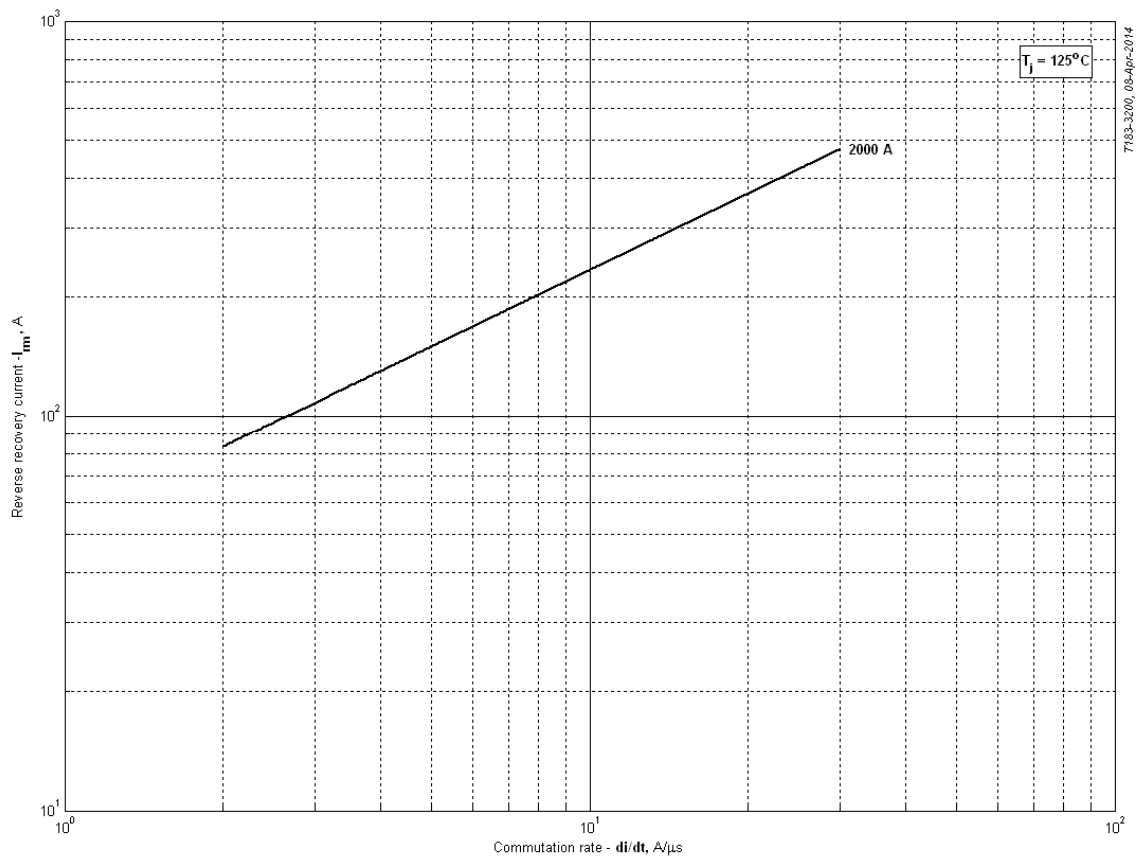


Fig 7 – Peak reverse recovery current, I_{rm}

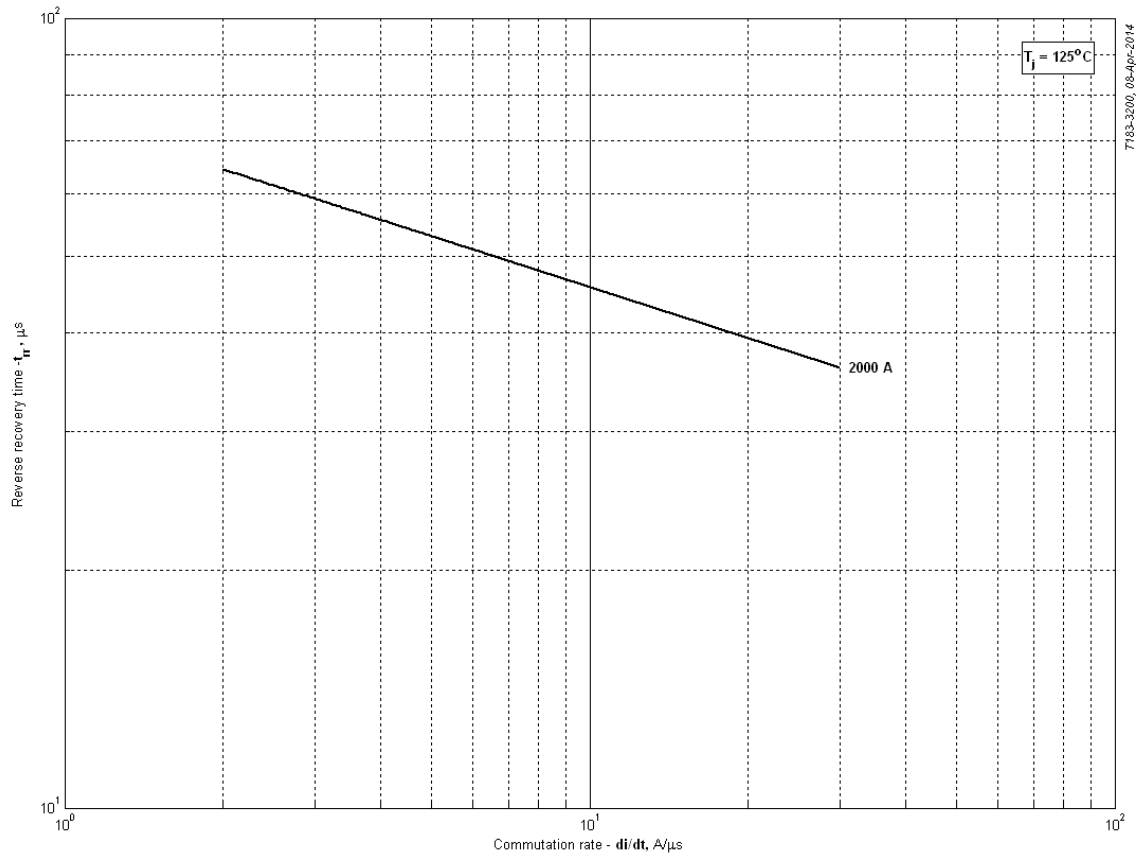


Fig 8 – Maximum recovery time, t_{tr} (linear)

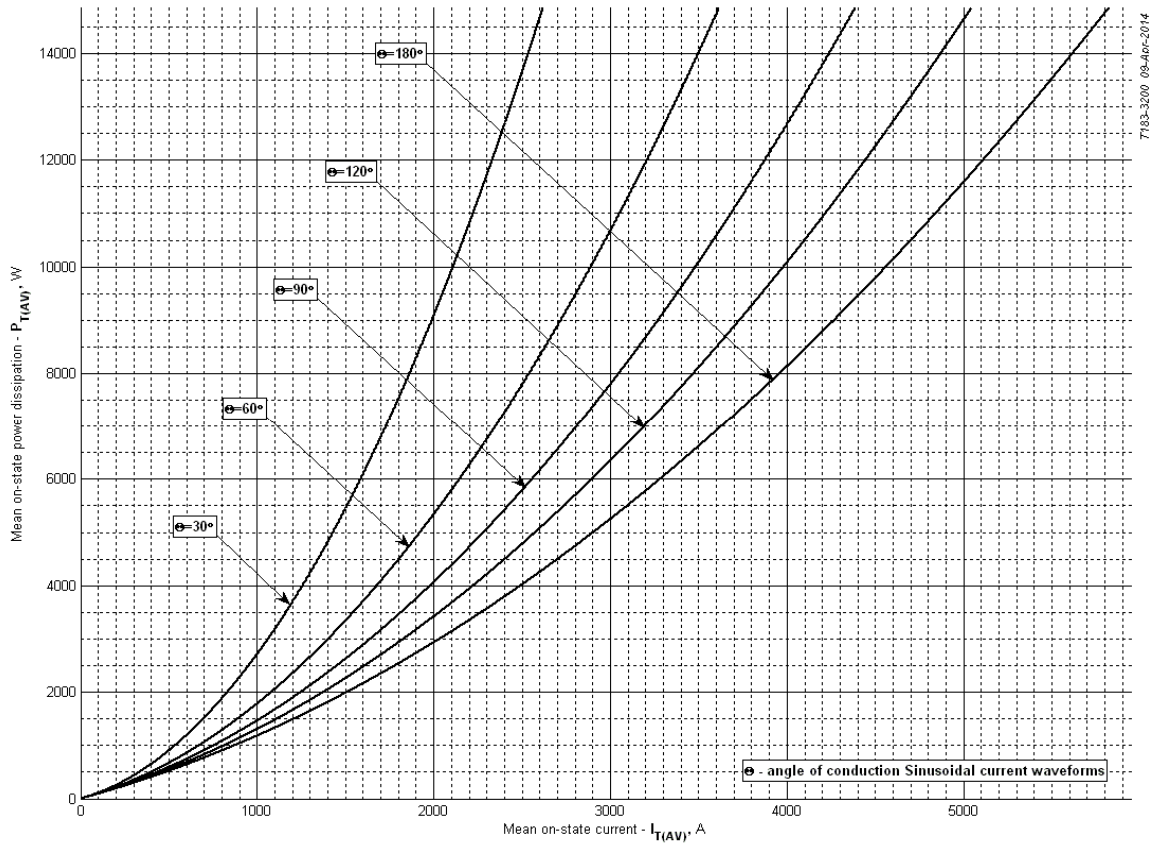


Fig 9 – On-state power loss (sinusoidal current waveforms)

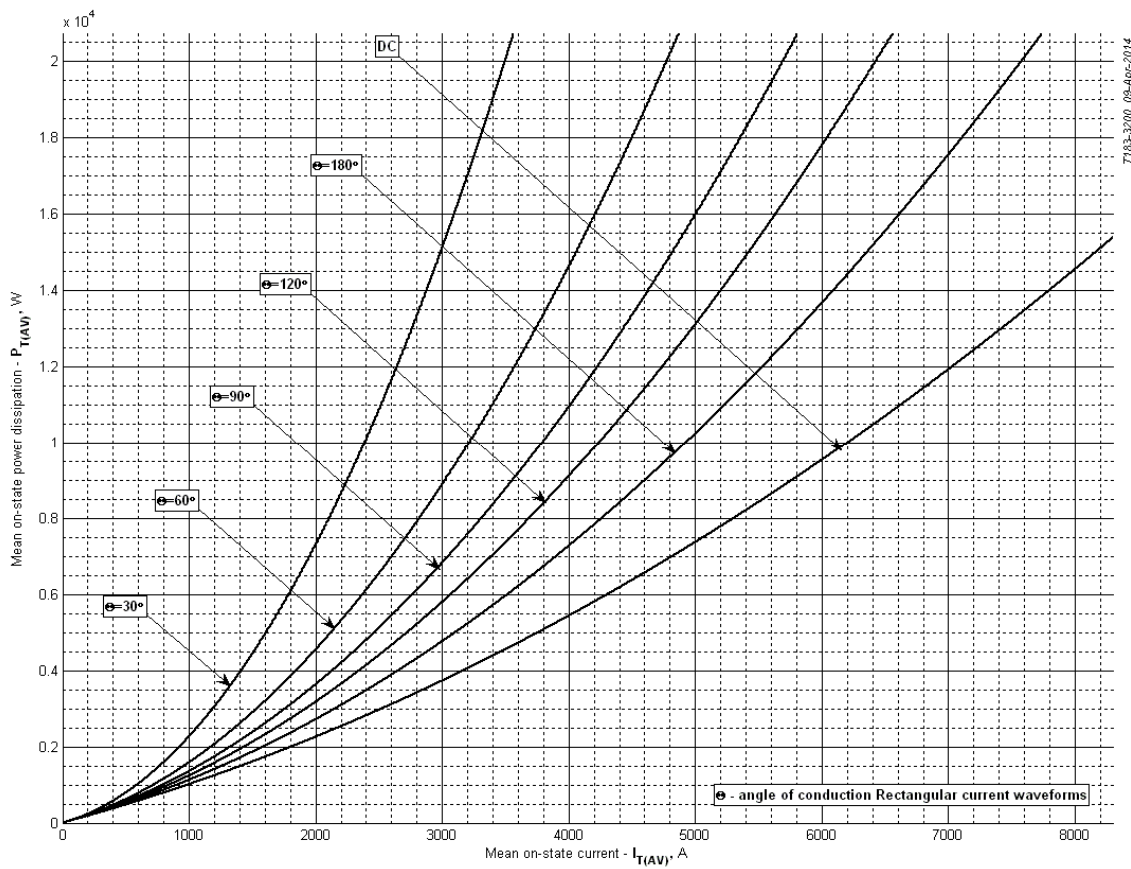


Fig 10 – On-state power loss (rectangular current waveforms)

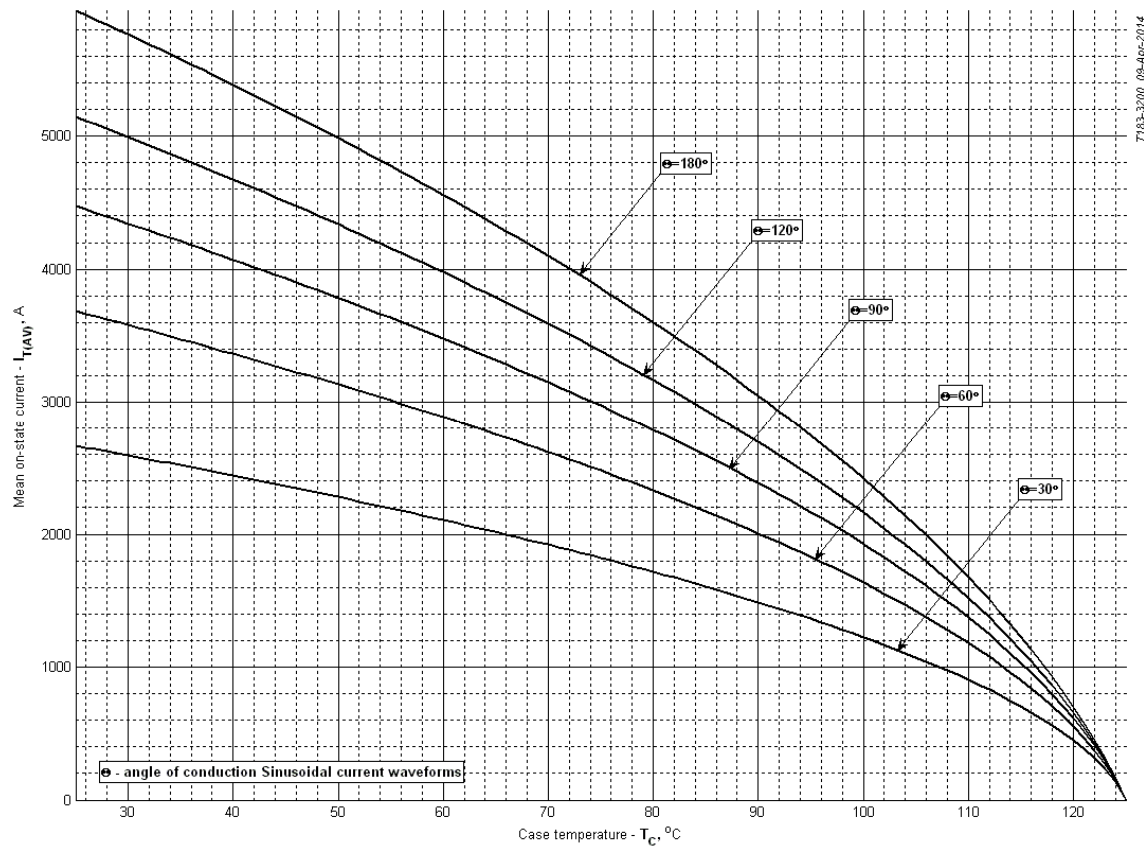


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

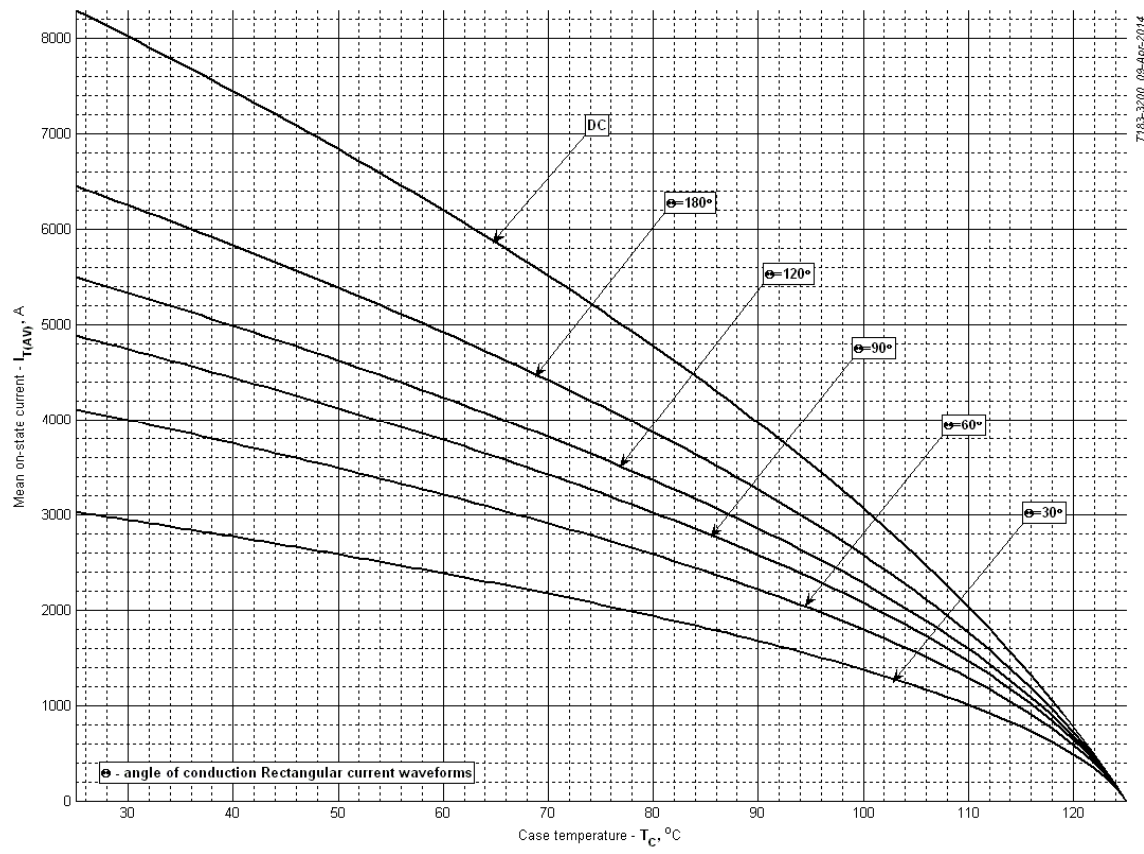


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

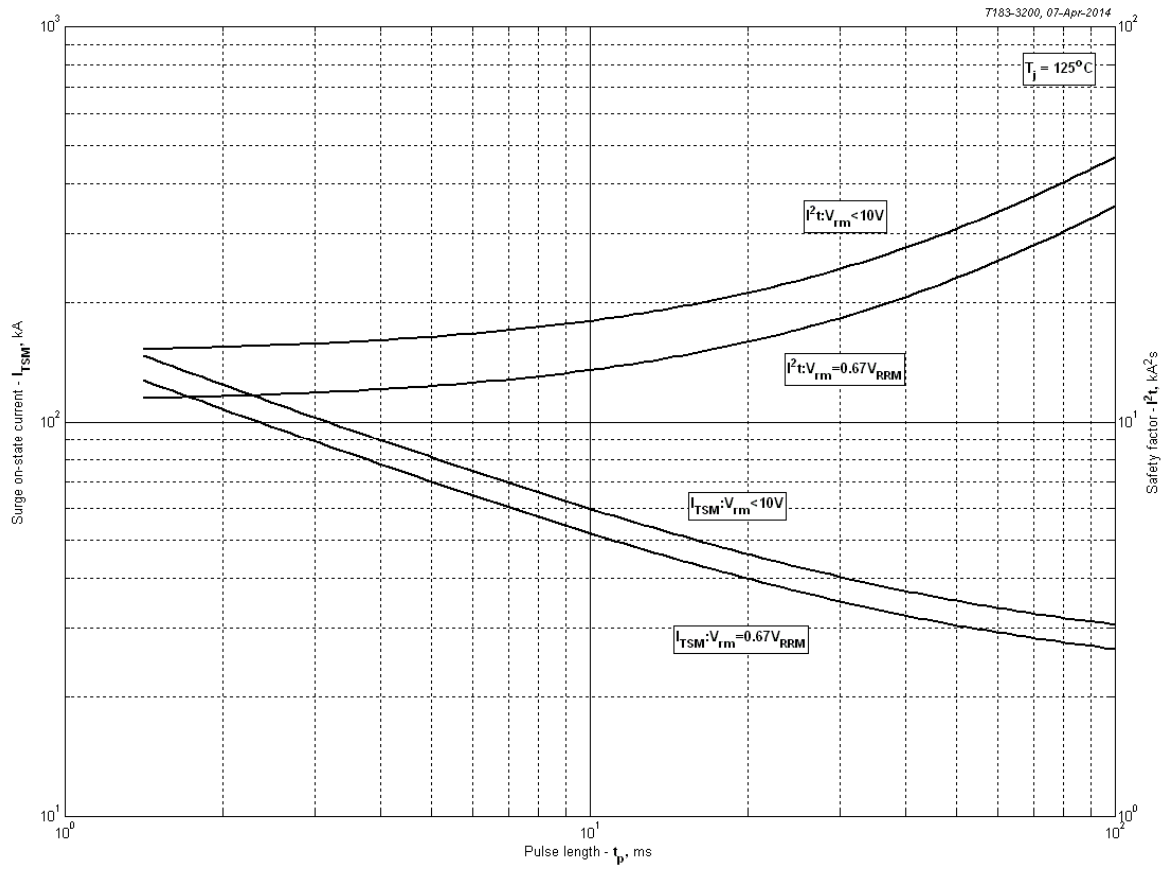


Fig 13 – Maximum surge and I^2t ratings

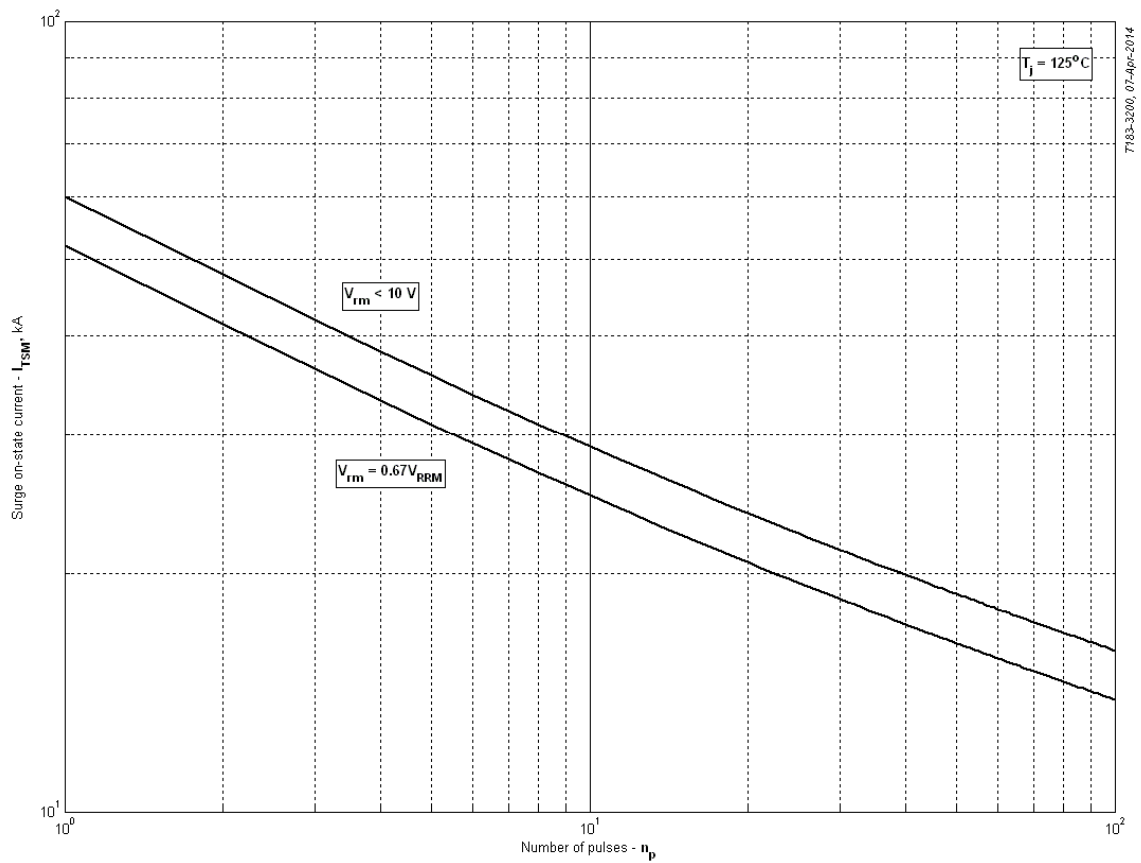


Fig 14 – Maximum surge ratings